DATA SHEET

PCD5008
FLEX™ Pager Decoder

Product specification
Supersedes data of 1997 Oct 27
File under Integrated Circuits, IC17

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- FLEX™ paging protocol signal processor
- 16 programmable user address words
- 16 fixed temporary addresses
- 1600, 3200 and 6400 bits/s decoding
- Any-phase or single-phase decoding
- Uses standard serial peripheral interface (SPI) in slave mode
- Allows low current power-down mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- FLEX™ fragmentation and group messaging support
- Real-time clock over-the-air update support
- Compatible with synthesized receivers
- Low battery indication (external detector)
- Low cost LQFP32 plastic package
- Operates using a 76.8 kHz crystal
- Very low power consumption
- Operates at low supply voltage.

2 APPLICATIONS

- Numeric FLEX™ pagers
- Alphanumeric FLEX™ pagers
- Remote metering
- Car security systems
- Personal digital assistants.

3 GENERAL DESCRIPTION

This data sheet describes the operation of the PCD5008 integrated paging decoder. It is fully compatible with the Motorola FLEXchip™ IC.

The PCD5008, also referred to as the decoder, simplifies implementation of a FLEX™ paging device, by being able to interface with several off-the-shelf paging receivers and host microcontrollers/processors. Its primary function is to process information received and demodulated from a FLEX™ radio paging channel, select messages addressed to the paging device and communicate the message information to the host.

Motorola FLEXstack™ software, installed on the product host processor, communicates with the PCD5008 and interprets the codewords that are passed to the host.

The PCD5008 operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low-power mode when no message is being received.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.8	2.2	3.6	V
I_{DD}	supply current	see Sections 10 and 12	–	6.4	–	µA
T_{amb}	operating ambient temperature		–25	+25	+70	°C
f_{EXTAL}	external clock frequency		–	76.8	–	kHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5008H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

6 BLOCK DIAGRAM

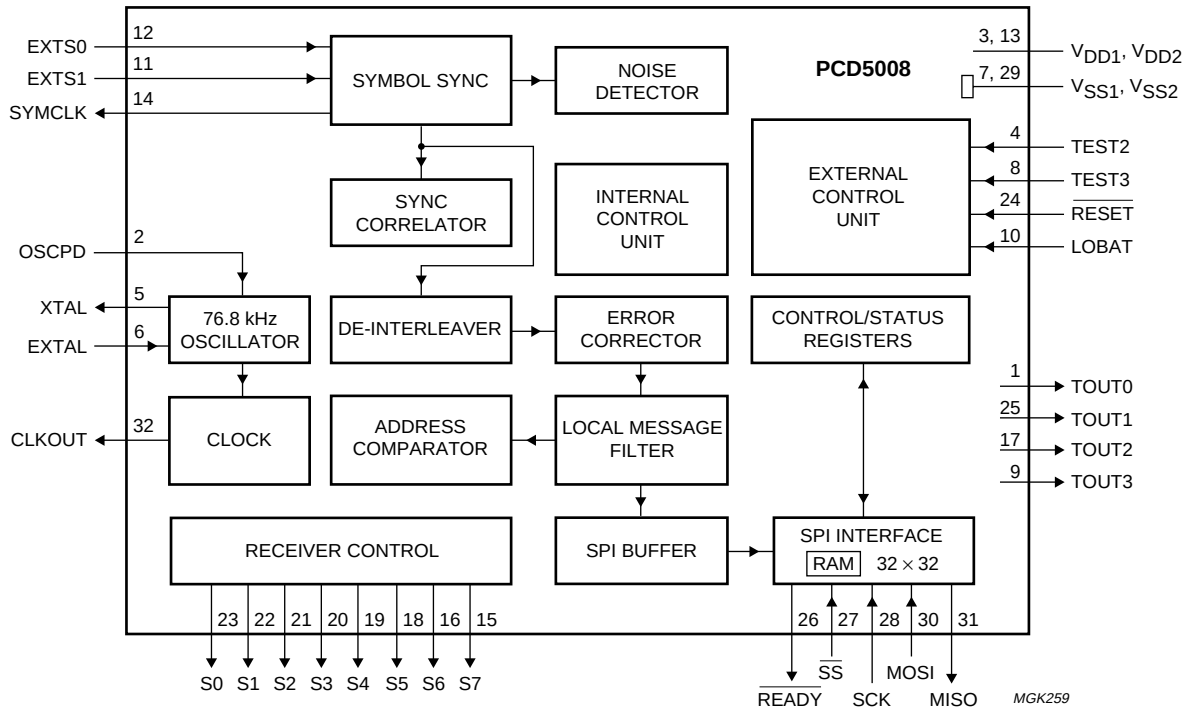


Fig.1 Functional block diagram for PCD5008 pager decoder.

7 PINNING

SYMBOL	PIN	I/O	PAD COORDINATE X/Y; note 1	DESCRIPTION
TOUT0	1	O	−1405/1088	3-state test output; note 2
OSCPD	2	I	−1405/816	internal oscillator power-down; connected to V_{SS} when using the internal oscillator, connected to V_{DD} when using an external source
V_{DD1}	3	–	−1405/563	supply voltage
TEST2	4	I	−1405/306	manufacturing test mode input pin; has to be connected to V_{SS}
XTAL	5	O	−1405/76	76.8 kHz crystal oscillator output
EXTAL	6	I	−1405/−404	76.8 kHz crystal oscillator input or external clock input
V_{SS1}	7	–	−1405/−648	ground supply
TEST3	8	I	−1405/−1104	manufacturing test mode input pin; has to be connected to V_{SS}
TOUT3	9	O	−1125/−1400	3-state test output; note 2
LOBAT	10	I	−863/−1400	low battery voltage detect input
EXTS1	11	I	−633/−1400	most significant bit (MSB) of the symbol currently being decoded
EXTS0	12	I	−398/−1400	least significant bit (LSB) of the symbol currently being decoded
V_{DD2}	13	–	134/−1400	supply voltage
SYMCLK	14	O	569/−1400	recovered symbol clock output
S7	15	O	829/−1400	receiver control output port, 3-state
S6	16	O	1084/−1400	receiver control output port, 3-state
TOUT2	17	O	1405/−1093	3-state test output; note 2
S5	18	O	1405/−718	receiver control output port, 3-state
S4	19	O	1405/−398	receiver control output port, 3-state
S3	20	O	1405/−93	receiver control output port, 3-state
S2	21	O	1405/202	receiver control output port, 3-state
S1	22	O	1405/502	receiver control output port, 3-state
S0	23	O	1405/812	receiver control output port, 3-state
$\overline{\text{RESET}}$	24	I	1405/1114	active LOW reset input
TOUT1	25	O	1051/1400	3-state test output; note 2
$\overline{\text{READY}}$	26	O	721/1400	output driven LOW when the PCD5008 is ready for an SPI packet
$\overline{\text{SS}}$	27	I	404/1400	slave select input for SPI communications
SCK	28	I	149/1400	serial clock input for SPI communications
V_{SS2}	29	–	−100/1400	ground supply
MOSI	30	I	−516/1400	data input for SPI communications
MISO	31	O	−789/1400	data output for SPI communications, 3-state
CLKOUT	32	O	−1084/1400	38.4 kHz clock output (derived from 76.8 kHz oscillator)

Notes

1. The pad coordinates are given in μm relating to the centre of the chip and are used in case of naked die delivery.
2. These test outputs may be either left unconnected or connected to V_{SS} in the application.

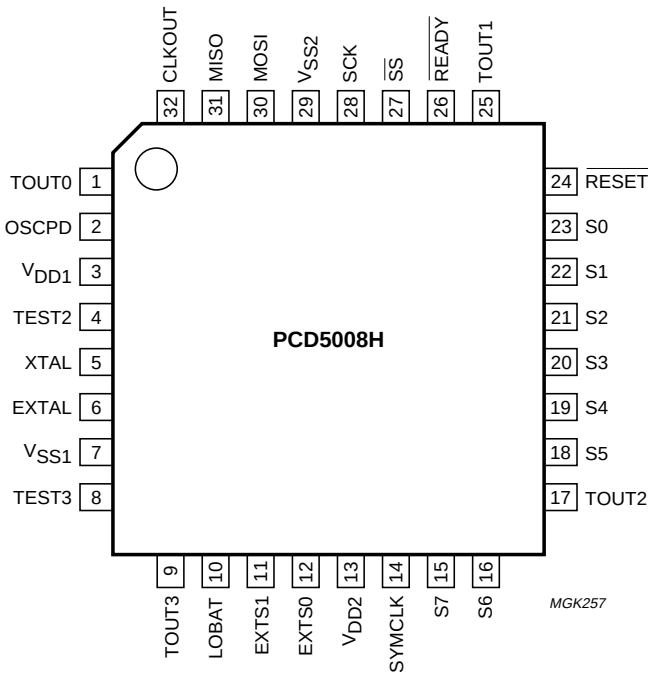


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 General

The PCD5008 simplifies implementation of a FLEX™ paging device by interfacing with off-the-shelf components such as a paging receiver and a microcontroller or microprocessor (called a host). The PCD5008 is fully compatible with FLEXstack™ software which provides a complete, platform independent, software driver for the PCD5008.

The PCD5008 fully supports all non-roaming aspects of the FLEX™ protocol (version G1.8), and can operate in either single-phase or any-phase mode. The PCD5008 supports FLEX™ dynamic grouping, allowing up to 16 temporary addresses to be enabled simultaneously. It is also capable of retrieving real time information from a FLEX™ channel.

The PCD5008 connects to any receiver capable of providing a 2-bit digital signal. The PCD5008 operates the paging receiver in an efficient power consumption mode. The PCD5008 has 8 receiver control lines used for warming up, operating and shutting down a receiver in stages.

The PCD5008 has the ability to detect a battery-low signal from an external detector during the receiver control sequences.

The PCD5008 carries out the following functions:

- Synchronises to a FLEX™ data stream
- Processes received, demodulated information
- Performs de-interleaving and error correction
- Selects calls addressed to the paging device using up to 16 programmable addresses
- Communicates the message information to the host.

The PCD5008 interfaces to a host through a serial peripheral interface (SPI). The host can then interpret the message information in an appropriate manner (numeric, alphanumeric, binary, etc.). This function is provided by the FLEXstack™ software.

The PCD5008 enables the host to operate in a low power mode when no message information for the paging device is being received. It has a 38.4 kHz clock output capable of driving other devices, and has a 1-minute timer that offers low-power support for a real-time clock function on the host. The host can use receiver control lines which are not required by the receiver as expansion ports to control other peripheral devices.

8.2 Clocking, reset and start-up

8.2.1 OSCILLATOR

The PCD5008 uses an inverting crystal oscillator.
The clock signal for the internal circuitry is derived via an amplifier from the oscillator input pin EXTAL. Alternatively, an external clock signal can be fed in at input pin EXTAL. In this case the internal oscillator can be disabled by pulling the OSCPD input pin HIGH.This reduces current consumption and routes EXTAL directly to the internal clock signal. When using a crystal, an external feedback resistor and the load capacitances need to be connected to pins EXTAL and XTAL (Fig.18). See Section 12 for the recommended crystal parameters and the specification of the oscillator transconductance to guarantee correct start-up.

8.2.2 RESET AND START-UP CONDITIONS

The PCD5008 is reset by pulling the $\overline{\text{RESET}}$ input LOW. After releasing the $\overline{\text{RESET}}$ by pulling it HIGH, the PCD5008 counts 76800 clock cycles (typically 1 second) before pulling $\overline{\text{READY}}$ LOW to indicate that the decoder is ready for configuration via the SPI.

See Fig.3 and Section 11 for the PCD5008 timing specifications when power is applied.

See Fig.4 and Section 11 for the PCD5008 timing specifications when it is reset.

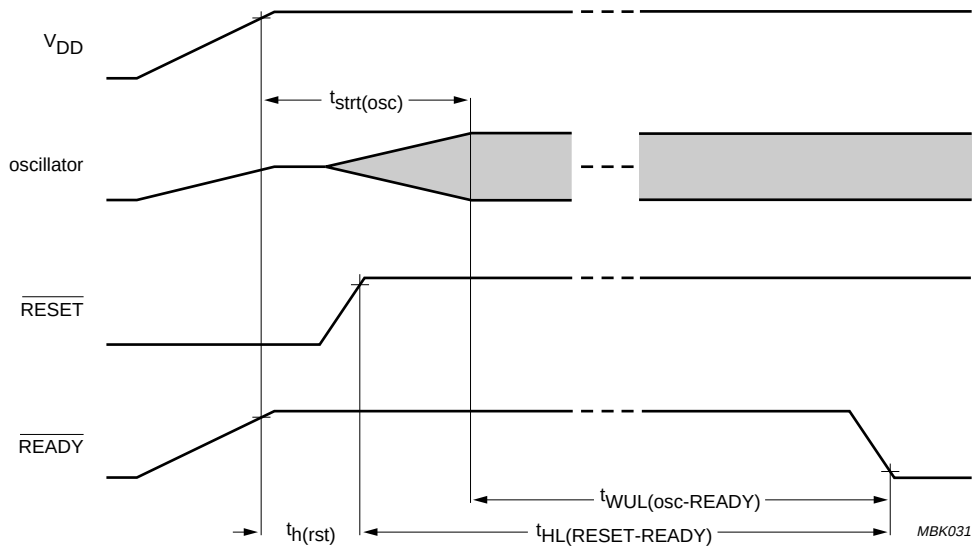


Fig.3 Start-up timing.

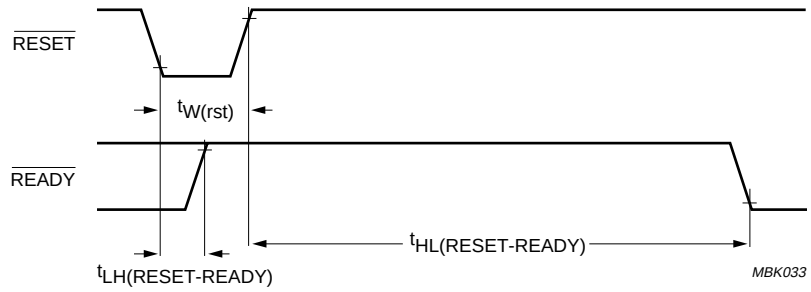


Fig.4 Reset timing.

8.3 Serial peripheral interface (SPI)

8.3.1 GENERAL

All data communication between the PCD5008 and the host is done via the SPI using 32-bit data packets at data rates up to 1 Mbits/s. SPI transfers are full-duplex and can be initiated by either the host which acts as the SPI master providing the data clock for packet transfer, or the PCD5008 as an SPI slave.

The host can send packets to configure or control the PCD5008 or a checksum packet to validate SPI communication (Section 8.4.2). The PCD5008 buffers data packets, relating to received data, into a 32 packet transmit buffer. The PCD5008 can send either a status packet, a part ID packet, or packets from the transmit buffer. In the event of a buffer overflow, the PCD5008 stops decoding and clears the transmit buffer.

8.3.2 SPI INTERCONNECT

Connection on the PCD5008 consists of a $\overline{\text{READY}}$ pin and 4 SPI pins ($\overline{\text{SS}}$, SCK, MOSI and MISO):

$\overline{\text{READY}}$: output signal; indicates that data is available from the PCD5008

$\overline{\text{SS}}$: SPI select; used as PCD5008 chip select

SCK: serial clock; output from the host used for clocking data

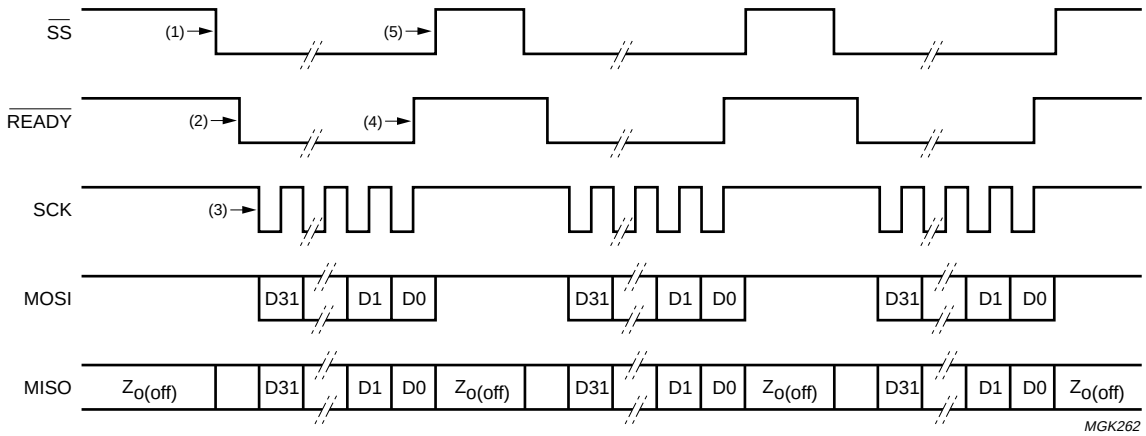
MOSI: master output slave input; data output from the host

MISO: master input slave output; data output from the PCD5008.

8.3.3 SPI TRANSFER INITIATED BY THE HOST

The following steps occur when the host initiates an SPI packet transfer, see Fig.5 for event timings:

1. The host selects the PCD5008 by driving the $\overline{SS}$ pin LOW.
2. The PCD5008 indicates that it is ready to start the SPI transfer by driving the $\overline{READY}$ pin LOW.
3. The host clocks each of the 32 bits of the SPI packet by pulsing SCK. Both the host and the PCD5008 sample data on the rising edge of SCK. Packets are sent MSB first.
4. The PCD5008 pulls the $\overline{READY}$ line HIGH, to indicate that the transfer is complete.
5. The host waits until the $\overline{READY}$ line is pulled HIGH, then de-selects the PCD5008 SPI by driving the $\overline{SS}$ pin HIGH.
6. The first 5 steps are repeated for each additional packet.



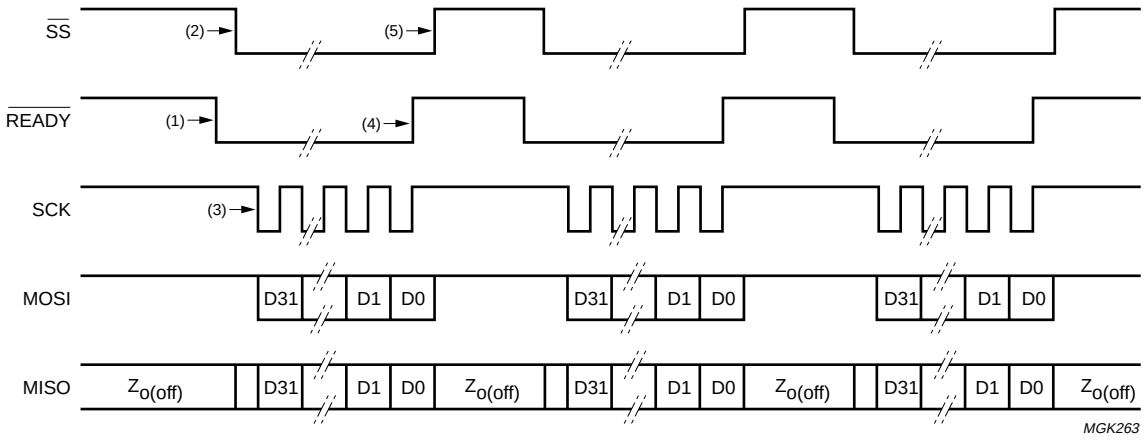
Numbers within parenthesis refer to sequence numbers, see Section 8.3.3.

Fig.5 Typical multiple SPI transfers initiated by the host.

8.3.4 SPI TRANSFER INITIATED BY THE DECODER

The following steps occur when the PCD5008 initiates an SPI packet transfer, see Fig.6 for event timings:

1. The PCD5008 initiates the SPI transfer by driving the $\overline{READY}$ pin LOW.
2. If the PCD5008 is not already selected, the host selects the PCD5008 SPI by driving the $\overline{SS}$ pin LOW.
3. The host clocks each of the 32 bits of the SPI packet by pulsing SCK. Both the host and the PCD5008 sample data on the rising edge of SCK. Packets are sent MSB first.
4. The PCD5008 pulls the $\overline{READY}$ line HIGH, to indicate that the transfer is complete.
5. The host may then either de-select the SPI interface of the PCD5008 (Fig.7) by driving the $\overline{SS}$ pin HIGH or maintain $\overline{SS}$ LOW to continue sending packets to the PCD5008.



Numbers within parenthesis refer to sequence numbers, see Section 8.3.4.

Fig.6 Typical multiple SPI transfers initiated by the PCD5008.

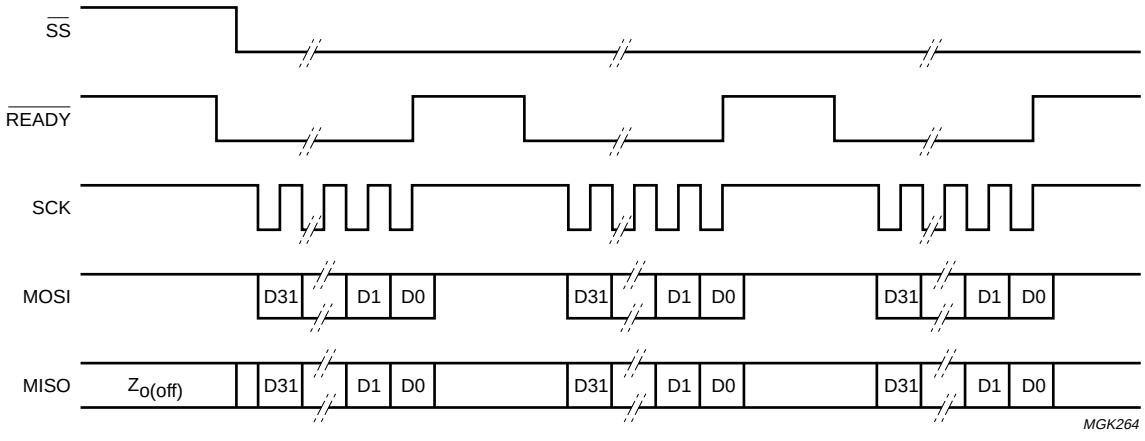


Fig.7 Multiple SPI transfers initiated by the PCD5008 with $\overline{SS}$ maintained LOW.

8.3.5 SPI PACKET FORMAT

SPI data packets consist of an 8-bit ID (byte 3), followed by 24 bits of information (byte 2 to byte 0). See Table 1, note that bit 7 of byte 3 is the first bit on the bus.

8.3.6 SPI TIMING

See Fig.8 and Chapter 11 for the timing specifications of the SPI.

Table 1 Packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	D31	D30	D29	D28	D27	D26	D25	D24
2	D23	D22	D21	D20	D19	D18	D17	D16
1	D15	D14	D13	D12	D11	D10	D9	D8
0	D7	D6	D5	D4	D3	D2	D1	D0

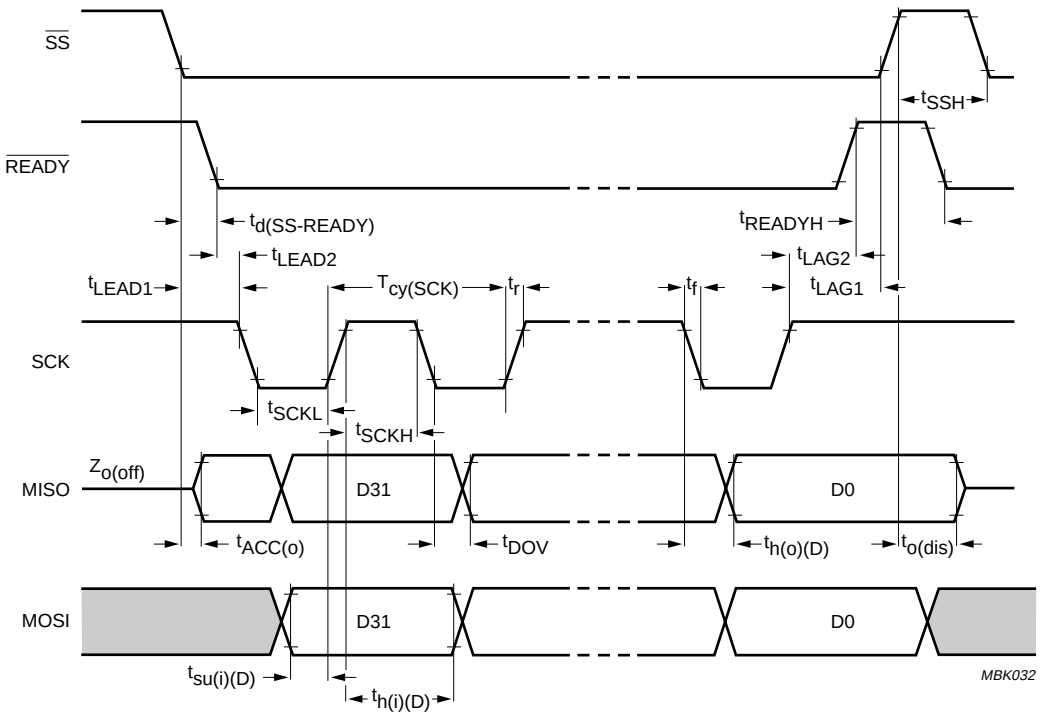


Fig.8 SPI timing.

8.3.7 HOST-TO-DECODER PACKETS OVERVIEW

This section summarises the packets which can be sent from the host to the decoder.

Table 2 Host-to-decoder packet ID map

PACKET		
ID (HEX)	**TYPE**	**SECTION**
00	checksum	8.4.6
01	configuration	8.4.4
02	control	8.4.7
03	all frame mode	8.8.3
04 to 0E	reserved (host should never send)	–
0F	receiver line control	8.5.7
10	receiver control configuration (off setting)	8.5.4
11	receiver control configuration (warm-up 1 setting)	8.5.5.3
12	receiver control configuration (warm-up 2 setting)	8.5.5.3
13	receiver control configuration (warm-up 3 setting)	8.5.5.3
14	receiver control configuration (warm-up 4 setting)	8.5.5.3
15	receiver control configuration (warm-up 5 setting)	8.5.5.3
16	receiver control configuration (3200 sps sync setting)	8.5.6.2
17	receiver control configuration (1600 sps sync setting)	8.5.6.2
18	receiver control configuration (3200 sps data setting)	8.5.6.2
19	receiver control configuration (1600 sps data setting)	8.5.6.2
1A	receiver control configuration (shut-down 1 setting)	8.5.8.1
1B	receiver control configuration (shut-down 2 setting)	8.5.8.1
1C to 1F	special (ignored by decoder)	–
20	frame assignment (frames 112 to 127)	8.6.7
21	frame assignment (frames 96 to 111)	8.6.7
22	frame assignment (frames 80 to 95)	8.6.7
23	frame assignment (frames 64 to 79)	8.6.7
24	frame assignment (frames 48 to 63)	8.6.7
25	frame assignment (frames 32 to 47)	8.6.7
26	frame assignment (frames 16 to 31)	8.6.7
27	frame assignment (frames 0 to 15)	8.6.7
28 to 77	reserved (host should never send)	–
78	user address enable	8.6.6
79 to 7F	reserved (host should never send)	–
80	user address assignment (user address 0)	8.6.6
81	user address assignment (user address 1)	8.6.6
82	user address assignment (user address 2)	8.6.6
83	user address assignment (user address 3)	8.6.6
84	user address assignment (user address 4)	8.6.6
85	user address assignment (user address 5)	8.6.6

PACKET		
ID (HEX)	**TYPE**	**SECTION**
86	user address assignment (user address 6)	8.6.6
87	user address assignment (user address 7)	8.6.6
88	user address assignment (user address 8)	8.6.6
89	user address assignment (user address 9)	8.6.6
8A	user address assignment (user address 10)	8.6.6
8B	user address assignment (user address 11)	8.6.6
8C	user address assignment (user address 12)	8.6.6
8D	user address assignment (user address 13)	8.6.6
8E	user address assignment (user address 14)	8.6.6
8F	user address assignment (user address 15)	8.6.6
90 to FF	reserved (host should never send)	–

8.3.8 DECODER-TO-HOST PACKETS OVERVIEW

This section summarises the packets which can be sent from the PCD5008 to the host (Table 3).

Table 3 Decoder-to-host packet ID map

PACKET		
ID (HEX)	**TYPE**	**SECTION**
00	block information word	8.7.9
01	address	8.7.2
02 to 57	vector or message (ID is word number in frame)	8.7.3, 8.7.8
58 to 7E	reserved	–
7F	status	8.4.9
80 to FE	reserved	–
FF	part ID	8.4.5

8.4 Configuration and synchronisation

8.4.1 GENERAL

After a reset, all configuration data has to be (re)loaded into the PCD5008 by the host using the SPI. PCD5008 features which do not change during operation are configured using the configuration packet (Section 8.4.4), the receiver control packets (Section 8.5) and the address configuration packets (Section 8.6). PCD5008 features which can be changed during operation are configured using the control packet. The checksum packet ensures proper communication between the host and the PCD5008.

8.4.2 SPI SECURITY ALGORITHM

The PCD5008 provides a security algorithm to verify correct SPI operation (Figs 9 and 10). The PCD5008 maintains a checksum register equal to the result of XORing the 24 data bits of every packet it receives, except the checksum packet 00H and special packets 1CH to 1FH. When the PCD5008 is reset, the internal checksum register is initialized to the 24 bit part ID defined in the part ID packet.

Immediately following a reset and whenever the host sends a packet other than a checksum packet, the SPI output of status and data (SPI transmit) is disabled. The PCD5008 then initiates SPI transfers continuously, sending the part ID packet (Section 8.4.5). Note that when SPI transmit is disabled all decoding and timing functions are unaffected. The SPI transmit can be enabled by sending a checksum packet for which the checksum value matches the checksum register.

Any checksum packets sent when the SPI transmit is enabled, are ignored by the PCD5008 irrespective of the value of the checksum packet data bits. Thus when the PCD5008 initiates an SPI transfer and the host has no data to send, the host should send the checksum packet so as not to disable the SPI transmit. The data in the checksum packet could be a null packet (32 bit stream of all zeros).

Sending a packet other than the checksum packet when the SPI transmit is enabled causes the SPI transmit to be disabled until a checksum packet is sent with the correct value. Thus when the host re-configures the PCD5008 after a reset, the SPI transmit is disabled until the host sends a checksum packet at the end of the configuration data, with the checksum value equal to the result of XORing together the data bits of each of the configuring packets and the data bits of the part ID packet.

If the SPI transmit is enabled and there is data in the transmit buffer, the PCD5008 initiates an SPI transfer sending a packet from its transmit buffer. The PCD5008 sends the status packet (which is not buffered) when the host initiates an SPI transfer and the transmit buffer is empty.

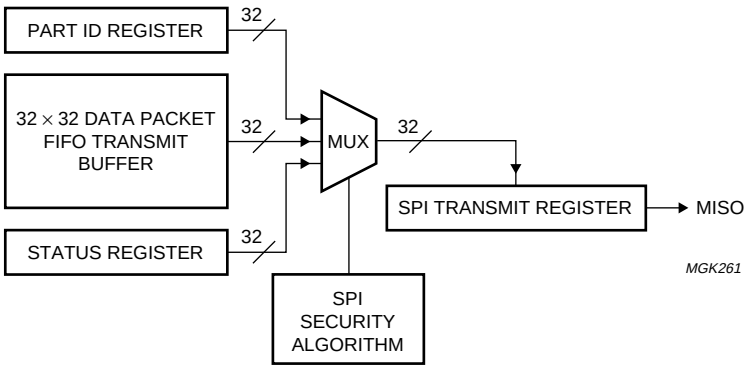


Fig.9 SPI transmit functional block diagram.

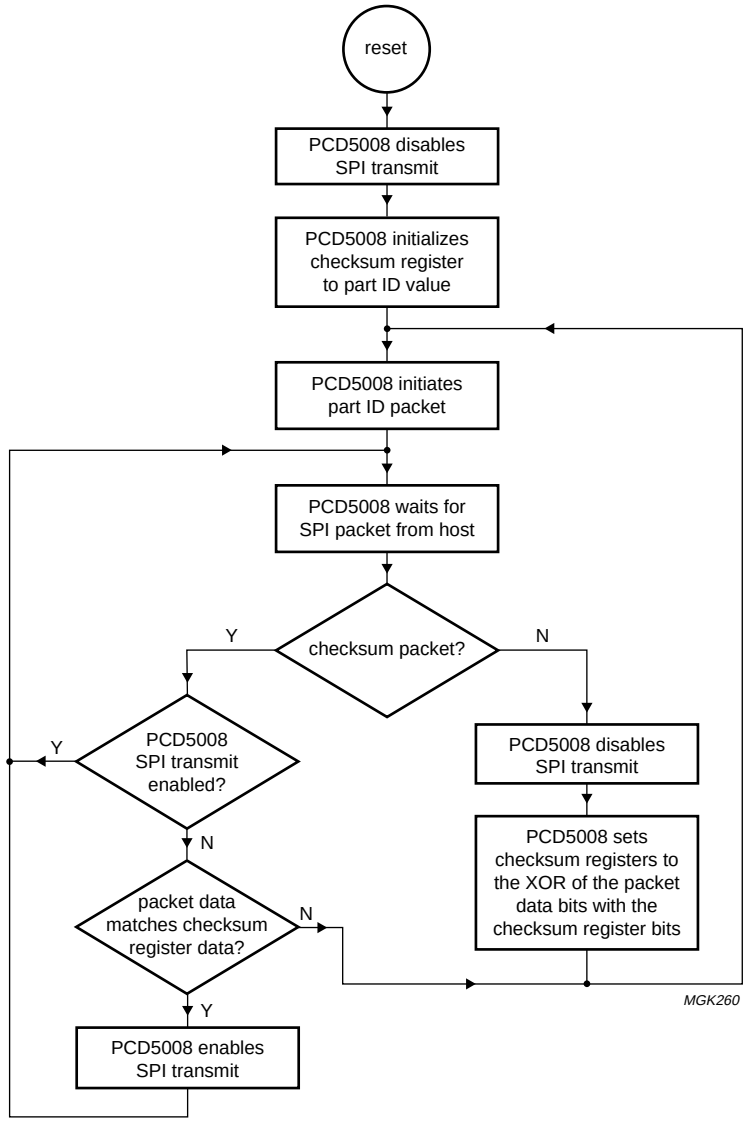


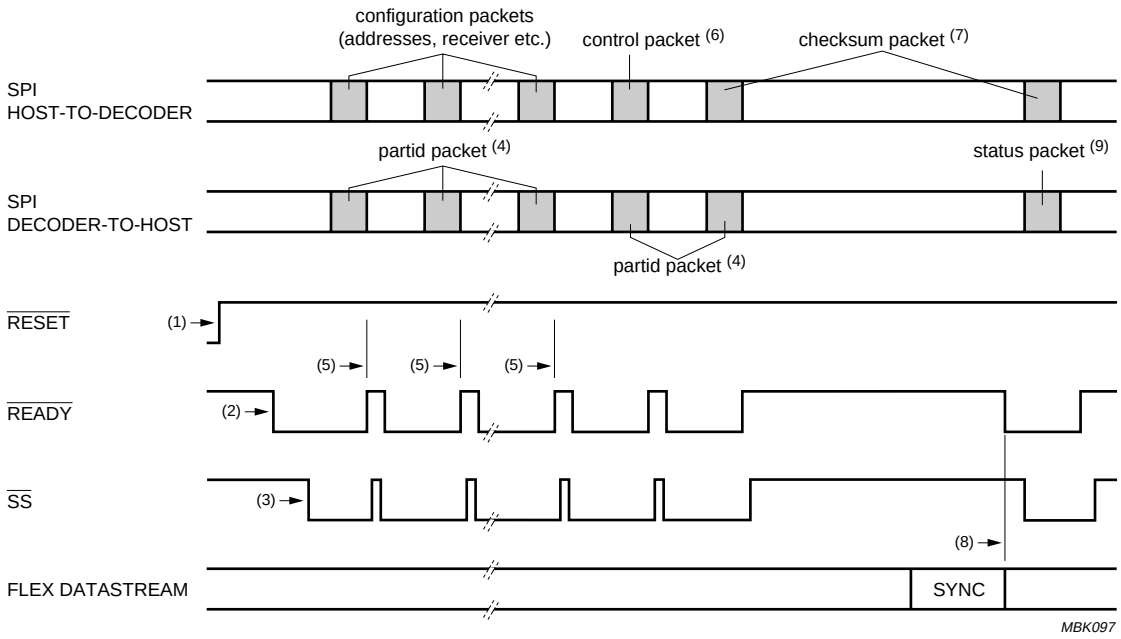
Fig.10 SPI security algorithm.

8.4.3 CONFIGURATION SEQUENCE

A typical configuration and synchronisation sequence would be as follows, see Fig.11 for event timings:

1. The PCD5008 is reset by the host.
2. After 1 second the PCD5008 interrupts the host to read the part ID by pulling the $\overline{\text{READY}}$ line LOW.
3. The host pulls $\overline{\text{SS}}$ LOW at the start of each SPI transfer and clocks out the part ID data.
4. The host configures the following aspects of PCD5008 operation:
   a) General configuration (Section 8.4.4)
   b) Receiver operation (Section 8.5)
   c) FLEX™ CAPCODE configuration (Section 8.6).

   The PCD5008 writes a part ID packet in response to each incoming packet.
5. At the end of each packet the PCD5008 pulls the $\overline{\text{READY}}$ line HIGH, and then LOW again to indicate that packet processing is complete.
6. The host writes a control packet to enable FLEX™ decoding in the PCD5008 (Section 8.4.7).
7. The host writes a checksum packet to enable SPI data output by the PCD5008 (Section 8.4.2).
8. On recognising a SYNC word, the PCD5008 synchronises to the channel.
9. The PCD5008 initiates an SPI transfer writing the status packet, indicating that it is now in synchronous mode.



Numbers within parenthesis refer to sequence numbers, see Section 8.4.3.

Fig.11 Typical configuration and synchronisation sequence.

8.4.4 CONFIGURATION PACKET (ID = 01H)

The configuration packet defines a number of different configuration options for the PCD5008. The PCD5008 ignores this packet when decoding is enabled, i.e. the ON bit in the control packet is set (Table 11).

OFD: oscillator frequency difference (Tables 4 and 5). These bits represent the maximum frequency difference between the 76.8 kHz oscillator (accounting for ageing, temperature variation, manufacturing tolerance etc.) and the worst case transmitter bit rate (specified in FLEX™ as ±25 parts per million (ppm), see Section 15.3.1). For example, if the transmitter tolerance is ±25 ppm and the 76.8 kHz oscillator tolerance is ±140 ppm, the transmitter-oscillator frequency difference is ±165 ppm and OFD should be cleared (300 ppm max.). Value after reset = 0. Note that configuring a smaller frequency difference in this packet results in lower power consumption due to higher receiver battery save ratios.

SME: synchronous mode enable (Table 5). When this bit is set, a status packet is sent automatically whenever the synchronous mode update (SMU) bit in the status packet is set. This happens whenever a change occurs in the synchronous mode (SM) status bit, which indicates that the decoder is synchronized to a FLEX™ data stream. The host can use the SM bit in the status packet as an in-range/out-of-range indication. Value after reset = 0.

MOT: maximum off time (Table 5). When this bit is set, the PCD5008 assumes that there can be up to 1 minute between transmitted frames on the paging system. When this bit is clear, the PCD5008 assumes that there can be up to 4 minutes between transmitted frames on the paging system. This setting is determined by the service provider. Value after reset = 0.

COD: clock output disable (Table 5). When this bit is clear, a 38.4 kHz signal is output on the CLKOUT pin. When this bit is set, the CLKOUT pin is driven HIGH. Note that setting and clearing this bit can cause pulses on the CLKOUT pin that are less than one half the 38.4 kHz period. Also note that when the clock output is enabled, the CLKOUT pin always outputs the 38.4 kHz signal even when the PCD5008 is in reset. Value after reset = 0.

MTE: minute timer enable (Table 5). When this bit is set, a status packet is sent at one minute intervals with the minute time-out (MT) bit in the status packet set. When this bit is clear, the internal 1-minute timer stops counting. See Section 8.4.8 for details of 1-minute timer operation. Value after reset = 0.

LBP: low battery polarity (Table 5). This bit defines the polarity of the PCD5008's LOBAT pin: When this bit is set, a HIGH at input LOBAT represents a low battery condition. The LB bit in the status packet is initialized to the inverse (i.e. inactive) value of the LBP bit when the PCD5008 is turned on (by setting the ON bit in the control packet). When the PCD5008 is turned on, the first low battery update in the status packet is sent to the host when a low battery condition is detected on the LOBAT pin. Value after reset = 0.

SP: signal polarity (Tables 5, 6 and 7). These bits set the polarity of EXTS1 and EXTS0 input signals. The polarity of the EXTS1 and EXTS0 bits is determined by the receiver design. Value after reset = 0.

Table 4 Maximum oscillator frequency difference

OFD_1	OFD_0	FREQUENCY DIFFERENCE (ppm)
0	0	±300
0	1	±150
1	0	±75
1	1	±0

Table 5 Configuration packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	OFD_1	OFD_0
1	0	0	0	0	0	0	SP_1	SP_0
0	SME	MOT	COD	MTE	LBP	0	0	0

Table 6 Input signal polarity

SP_1	SP_0	SIGNAL POLARITY	
		EXTS1	EXTS0
0	0	normal	normal
0	1	normal	inverted
1	0	inverted	normal
1	1	inverted	inverted

Table 7 FLEX™ 4 level FSK modulation selection

EXTS1	EXTS0	FSK MODULATION AT SP = 0,0 (Hz)
1	0	+4800
1	1	+1600
0	1	−1600
0	0	−4800

8.4.5 PART ID PACKET (ID = FFH)

The part ID packet is output by the PCD5008 SPI whenever the SPI transmit is disabled due to the checksum feature.

MDL: model (Table 8). The PCD5008 model value is 0.

CID: compatibility ID (Table 8). This value describes other parts with the same model number, which are compatible with this part. The PCD5008 compatibility value is 1. Devices which implement a superset of PCD5008 functionality have MDL cleared and CID_0 set.

REV: revision (Table 8). This identifies the manufacturing version of the PCD5008. For the PCD5008 the value is 6. Compatible parts have values in the range 0 to 5.

8.4.6 CHECKSUM PACKET (ID = 00H)

See Table 9 for checksum packet bit assignment.

CV: checksum value (24 bits), see Section 8.4.2.

Table 8 Part ID packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	1	1	1	1	1	1	1	1
2	MDL_1	MDL_0	CID_{13}	CID_{12}	CID_{11}	CID_{10}	CID_9	CID_8
1	CID_7	CID_6	CID_5	CID_4	CID_3	CID_2	CID_1	CID_0
0	REV_7	REV_6	REV_5	REV_4	REV_3	REV_2	REV_1	REV_0

Table 9 Checksum packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	0
2	CV_{23}	CV_{22}	CV_{21}	CV_{20}	CV_{19}	CV_{18}	CV_{17}	CV_{16}
1	CV_{15}	CV_{14}	CV_{13}	CV_{12}	CV_{11}	CV_{10}	CV_9	CV_8
0	CV_7	CV_6	CV_5	CV_4	CV_3	CV_2	CV_1	CV_0

8.4.7 CONTROL PACKET (ID = 02H)

The control packet defines a number of different control bits for the PCD5008.

FF: force frame 0 to 7 (Table 11). When set, each of these bits forces the PCD5008 to decode one of the FLEX™ frames 0 to 7 irrespective of the system collapse value (for details of collapse values see Section 8.6.2). For example, if the system collapse causes the PCD5008 to decode frames 0, 32, 64 and 96, setting FF_2 causes the PCD5008 to also decode FLEX™ frame 2. This may be used to acquire transmitted time information. Value after reset = 0.

SPM: single phase mode (Table 11). When this bit is set, the PCD5008 decodes only one of the transmitted phases. When this bit is clear, the PCD5008 decodes all transmitted phases. This value is determined by the CAPCODE (Section 8.6). A change to this bit while the PCD5008 is on does not take effect until the next block 0 of a frame. Value after reset = 0.

PS: phase select (Tables 10 and 11). When the SPM bit is set, these bits define which phase the PCD5008 shall decode. This value is determined by the CAPCODE (Section 8.6). A change to these bits, while the PCD5008 is on, does not take effect until the next block 0 of a frame. Value after reset = 0.

Table 10 Phase selection (PS bits)

PS_1	PS_0	DECODED PHASE (BASED ON FLEX™ DATA RATE)		
		1600 bits/s	3200 bits/s	6400 bits/s
0	0	A	A	A
0	1	A	A	B
1	0	A	C	C
1	1	A	C	D

SBI: send block information words (BIW) 2 to 4 (Table 11). When this bit is set, BIWs with time and date information and BIWs received in error are sent to the host, (Section 8.7.9). Value after reset = 0.

MTC: minute timer clear (Table 11). Setting this bit causes the 1-minute timer to restart from 0 (Section 8.4.8).

ON: turn on decoder (Table 11). When this bit is set, the PCD5008 decodes FLEX™ signals. If this bit is cleared, signal processing stops. However, to assure proper operation, the PCD5008 requires that it be set into asynchronous mode when turned off. To achieve that the following sequence must be used:

1. Send control packet with ON bit clear (decoder off)
2. Send control packet with ON bit set (decoder on)
3. Send control packet with ON bit clear (decoder off).

Timing between these steps is specified below and is measured from the positive edge of the last clock of one packet to the positive edge of the last clock of the next packet.

- The minimum time between steps 1 and 2 is the greater of 2 ms or the programmed shut-down time.
  The programmed shut-down time is the sum of all of the times programmed in the used receiver shut-down settings packets.
- There is no maximum time between steps 1 and 2
- The minimum time between steps 2 and 3 is 2 ms
- The maximum time between steps 2 and 3 is the programmed warm-up time minus 2 ms.
  The programmed warm-up time is the sum of all the times programmed in the used receiver warm-up settings packets.

8.4.8 OPERATING THE 1-MINUTE TIMER

The PCD5008 provides a 1-minute timer which allows the host to implement a time-of-day function while maintaining low-power operation. The 1-minute timer is enabled using the MTE bit in the configuration packet (Section 8.4.4). When the 1-minute timer is enabled, a status packet is sent at 1-minute intervals with the MT bit set (Section 8.4.9). When the MTE bit is clear, the internal 1-minute timer stops counting. When the host sends a control packet with MTC bit set, the 1-minute timer restarts from 0. This allows accurate setting of a time-of-day function.

Table 11 Control packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	1	0
2	FF_7	FF_6	FF_5	FF_4	FF_3	FF_2	FF_1	FF_0
1	0	SPM	PS_1	PS_0	0	0	0	0
0	0	SBI	0	MTC	0	0	0	ON

8.4.9 STATUS PACKET (ID = 7FH)

The status packet contains various types of information that the host may require and is sent to the host:

- Whenever the PCD5008 is polled and has no other data to send
- On events for which the PCD5008 is configured to send the status packet (Sections 8.4.4 and 8.4.7). In this case, the PCD5008 prompts the host to read a status packet for the following conditions:
  - SMU bit in the status packet and the SME bit in the configuration packet are set
  - MT bit in the status packet and the MTE bit in the configuration packet are set
  - EOF bit in the status packet is set
  - LBU bit in the status packet is set
  - BOE bit in the status packet is set.

FIV: frame information valid (Table 12). This bit is set, when a valid frame information word has been received since becoming synchronous to the system and the f and c fields contain valid values. If this bit is clear, no valid frame information words have been received since the PCD5008 became synchronous to the system. This value changes from 0 to 1 at the end of block 0 (Fig.17) of the frame in which the first frame information word was properly received. It is cleared when the PCD5008 goes into asynchronous mode (see SM bit below). This bit is initialized to 0 when the PCD5008 is reset and when the PCD5008 is turned off by clearing the ON bit in the control packet.

f: current frame number (Table 12). This value is updated every frame regardless of whether the PCD5008 needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

c: current system cycle number (Table 12). This value is updated every frame regardless of whether the PCD5008 needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SM: synchronous mode (Table 12). This bit is set, when the PCD5008 is synchronous to the system.
The PCD5008 sets this bit when the first synchronization words are received. It clears this bit when synchronisation to the FLEX™ signal is lost. This bit is initialized to 0 when the PCD5008 is reset and when it is turned off by clearing the ON bit in the control packet.

SMU: synchronous mode update (Table 12). This bit is set if the SM bit has been updated in this packet. After the PCD5008 has been turned on, this bit is set when the first synchronization words are found (SM changes to 1) or when the first synchronization search period (meaning the receiver is active during this time) expires (SM stays 0), after the PCD5008 is turned on. The latter condition gives the host the option of assuming the paging device is in range when it is turned on, and displaying out-of-range only after the initial search period expires. After the initial synchronous mode update, the SMU bit is set whenever the PCD5008 switches from/to synchronous mode. The bit is cleared when read. Changes in the SM bit due to turning off the PCD5008 does not set the SMU bit. This bit is initialized to 0 when the PCD5008 is reset.

LB: low battery (Table 12). Set to the value last read from the LOBAT pin. The host controls when the LOBAT pin is read via the receiver control packets. This bit is initialized to 0 at reset. It is also initialized to the inverse of the LBP bit in the configuration packet, when the PCD5008 is turned on, by setting the ON bit in the control packet.

LBU: low battery update (Table 12). This bit is set if the value on two consecutive reads of the LOBAT pin yielded different results. The bit is cleared when read. The host controls when the LOBAT pin is read via the receiver control packets. Changes in the LB bit due to turning on the PCD5008 do not cause the LBU bit to be set. This bit is initialized to 0 when the PCD5008 is reset.

MT: minute time-out (Table 12). Set if one minute has elapsed. The bit is cleared when read. This bit is initialized to 0 when the PCD5008 is reset.

EOF: end of frame (Table 12). Set when the PCD5008 is in all frame mode (AFM) (Section 8.8.3), and the end of the frame has been reached. The PCD5008 is in the AFM if the AFM enable counter is non-zero, if any temporary address enabled (TAE) counter is non-zero (Section 8.8.3) or if the FAF bit in the AFM packet is set. The bit is cleared when read and initialized to 0 when the PCD5008 is reset.

BOE: buffer overflow error (Table 12). Set when information has been lost owing to slow host response time. When the PCD5008 detects that its SPI transmit buffer has overflowed, it clears the transmit buffer, turns off decoding by clearing the ON bit in the control packet, and sets this bit. The bit is cleared when read. This bit is initialized to 0 when the PCD5008 is reset.

x: unused bits (Table 12). The value of these bits is not guaranteed.

8.5 Receiver control interface

8.5.1 General

The PCD5008 has 8 programmable receiver control lines, S0 to S7. The host can program via SPI packets what setting is applied to the receiver control lines, the duration of warm-up and shut-down stages and the polling of the LOBAT pin. This programmability allows the PCD5008 to interface with many off-the-shelf receiver ICs. Note that these packets are ignored when sent while decoding is enabled (ON bit is set in the control packet).

8.5.2 Low battery detection

The PCD5008 can be configured to poll the LOBAT pin at the end of every receiver control setting. This check can be enabled or disabled for each receiver control setting. If the poll is enabled for a setting, the pin is read just before the PCD5008 activates the next setting on the receiver control lines. The PCD5008 sends a status packet whenever the value differs from the previous time that the LOBAT pin was polled.

8.5.3 Receiver settings at reset

The receiver control ports are 3-state outputs which are set to high impedance when the PCD5008 is reset, until the corresponding FRS bit in the receiver line control packet is set or the PCD5008 is turned on for the first time after a reset (by setting the ON bit in the control packet). This allows the designer to force the receiver control lines to the receiver off setting with external pull-up or pull-down resistors before the host can configure these settings in the PCD5008.

8.5.4 Receiver off state (ID = 10H)

The receiver off state is configured by the receiver off setting packet (Table 13), which defines the settings to be applied when the PCD5008 decides to switch the receiver off.

LBC: low battery check (Table 13). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving the receiver off state. Value after reset = 0.

CLS: control line setting (Table 13). This is the value to be output on the receiver control lines for the receiver off state. Value after reset = 0.

ST: step time (Table 13). This sets the duration of the warm-up off time. The setting is in steps of 625 μs. Valid values are 625 μs (ST = 01H) to 159.375 ms (ST = FFH). Value after reset = 01H.

Table 12 Status packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	1	1	1
2	FIV	f_6	f_5	f_4	f_3	f_2	f_1	f_0
1	SM	LB	x	x	c_3	c_2	c_1	c_0
0	SMU	LBU	x	MT	x	EOF	x	BOE

Table 13 Receiver off setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	0	0	0	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

8.5.5 RECEIVER WARM-UP SEQUENCES

8.5.5.1 Normal receiver warm-up sequence

The PCD5008 allows for up to 6 steps associated with warming up the receiver. When the PCD5008 turns on the receiver while decoding, it starts the warm-up sequence 160 ms before it requires valid signals at the EXTS1 and EXTS0 input pins.

1. The PCD5008 leaves the receiver control lines in the off state for the programmed warm-up off time.
2. The first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting.
3. Subsequent warm-up settings are applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found.
4. At the end of the last used warm-up setting, the 1600 symbols per second (sps) sync setting or the 3200 sps sync setting is applied to the receiver control lines depending on the PCD5008 current state.

The PCD5008 must be configured such that the sum of all of the used warm-up times and the warm-up off time does not exceed 160 ms.

If it exceeds 160 ms, the PCD5008 executes the receiver shut-down sequence 160 ms after the start of the warm-up off time. If the sum of all of the used warm-up times and the warm-up off times is less than 160 ms, the receiver remains in the 1600 sps sync setting or the 3200 sps sync setting from the end of the last used warm-up setting until valid signals are expected (160 ms after the start of the warm-up off time). Figure 12 shows the receiver warm-up sequence while decoding, when all warm-up settings are enabled.

8.5.5.2 First receiver warm-up sequence

When the PCD5008 is turned on by setting the ON bit in the control packet, the receiver warm-up sequence differs from the sequence described in Section 8.5.5.1. After the ON bit is set no receiver warm-up off time is applied, instead the PCD5008 immediately begins to apply the receiver warm-up settings. When a disabled warm-up setting is found, the decoder applies 3200 sps sync setting to the receiver control lines. The decoder then expects valid signals after the 3200 sps sync warm-up time. Figure 13 shows the receiver warm-up sequence when the PCD5008 is first turned on and when all warm-up settings are enabled.

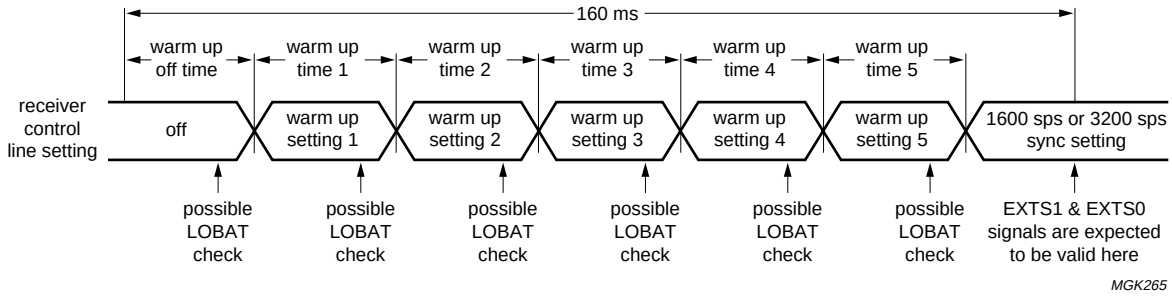


Fig.12 Receiver warm-up sequence while decoding.

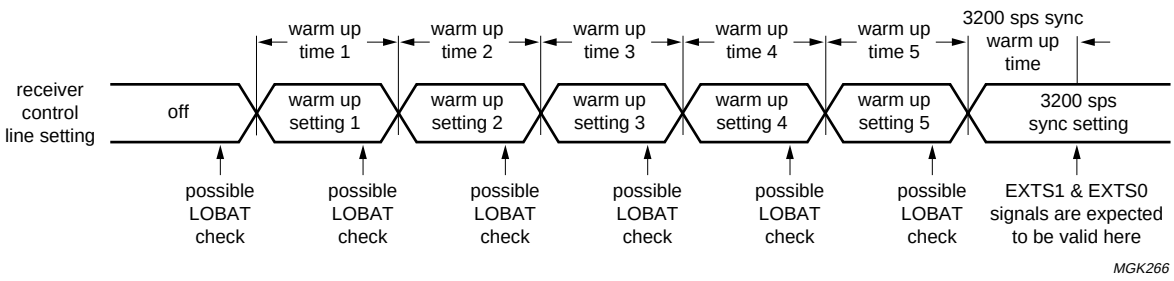


Fig.13 First receiver warm-up sequence after turning decoding on.

8.5.5.3 Receiver warm-up setting packets (ID = 11H to 15H)

CLS: control line setting (Table 15). This is the value to be output on the receiver control lines (S0 to S7) for this receiver warm-up state. Value after reset = 0.

SE: step enable (Table 15). The receiver setting is enabled when the bit is set. If the bit is cleared then that step in the receiver warm-up sequence is disabled and all following steps are ignored. Value after reset = 0.

LBC: low battery check (Table 15). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver warm-up state. Value after reset = 0.

ST: step time (Table 15). This sets the duration time for receiver warm-up until the next receiver state. The setting is in 625 μs steps and valid values are:

625 μs (ST = 01H) to 79.375 ms (ST = 7FH).

Value after reset = 01H.

s: setting number, see Tables 14 and 15 for the s names and values and location in the receiver warm-up packet.

Table 14 Receiver warm-up setting numbers

s_3	s_2	s_1	s_0	SETTING NAME
0	0	0	1	warm-up 1
0	0	1	0	warm-up 2
0	0	1	1	warm-up 3
0	1	0	0	warm-up 4
0	1	0	1	warm-up 5

Table 15 Receiver warm-up setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

8.5.6 ACTIVE RECEIVER STATES

8.5.6.1 General

In addition to the warm-up and shut-down states, the PCD5008 has four active receiver states. When these settings are applied to the receiver control lines, the PCD5008 is decoding the EXTS1 and EXTS0 input signals. The timing of these signals and their duration depends on the FLEX™ data stream. Because of this, there is no time setting associated with these settings (with the exception of the 3200 sps sync setting).

The four settings are as follows:

1600 sps sync setting: applied when the PCD5008 searches for a 1600 sps signal.

3200 sps sync setting: applied when the PCD5008 searches for a 3200 sps signal.

1600 sps data setting: applied after the PCD5008 has found the C or $\overline{C}$ sync word in the sync 2 section of a 1600 sps frame.

3200 sps data setting: applied after the PCD5008 has found the C or $\overline{C}$ sync word in the sync 2 section of a 3200 sps frame.

Figure 14 shows some examples of how these settings are used in the PCD5008.

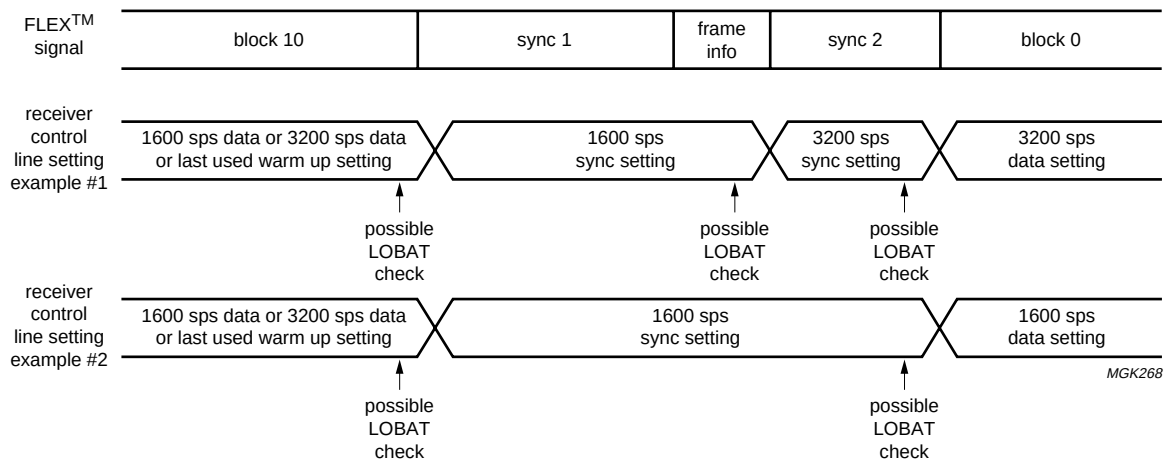


Fig.14 Examples of receiver control transitions.

8.5.6.2 Receiver on setting packets (ID = 16H to 19H)

LBC: low battery check (Table 17). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver sync setting state. Value after reset = 0.

CLS: control line setting (Table 17). This is the value to be output on the receiver control lines for this receiver sync setting state. Value after reset = 0.

ST: step time (Table 17). This sets the waiting time, before expecting good signals at EXTS1 and EXTS0 at the end of the warm-up sequence, after turning decoding on. The setting is in steps of 625 µs. Valid values are: 625 µs (ST = 01H) to 79.375 ms (ST = 7FH). Value after reset = 01H.

LBC: low battery check (Table 18). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver on state. Value after reset = 0.

CLS: control line setting (Table 18). This is the value to be output on the receiver control lines (S0 to S7) for this receiver on state. Value after reset = 0.

s: setting number, see Tables 16 and 18 for the s names and values and location in the receiver on setting packet.

Table 16 s names and values

s_3	s_2	s_1	s_0	SETTING NAME
0	1	1	1	1600 sps sync
1	0	0	0	3200 sps data
1	0	0	1	1600 sps data

8.5.7 FORCING RECEIVER LINES (ID = 0FH)

This packet (Table 19) enables host control over the receiver control line (S0 to S7) settings in all modes except reset. In reset, the receiver control lines are high impedance.

FRS: force receiver setting (Table 19). Setting a bit causes the associated CLS bit in this packet to override the internal receiver control settings on the corresponding receiver control line. Clearing a bit returns control of the corresponding receiver control line to the PCD5008. Value after reset = 0.

CLS: control line setting (Table 19). This bit setting is applied to the corresponding receiver control line if the associated FRS bit is set in this packet. Value after reset = 0.

Table 17 3200 sps sync setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	0	1	1	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

Table 18 Receiver on setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	0	0	0	0	0	0

Table 19 Receiver line control packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	1	1	1	1
2	0	0	0	0	0	0	0	0
1	FRS_7	FRS_6	FRS_5	FRS_4	FRS_3	FRS_2	FRS_1	FRS_0
0	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0

8.5.8 RECEIVER SHUT-DOWN SEQUENCE

The PCD5008 allows up to 3 steps associated with shutting down the receiver. When the PCD5008 decides to turn off the receiver, the first shut-down setting, if enabled, is applied to the receiver control lines for the corresponding shut-down time. At the end of the last used shut-down time, the receiver off setting is applied to the receiver control lines. If the first shut-down setting is not enabled, the PCD5008 switches directly from the receiver on to the receiver off setting.

Figure 15 shows the receiver shut-down sequence when all shut-down settings are enabled. If the receiver is on or being warmed up when the decoder is turned off (by clearing the ON bit in the control packet), the PCD5008 immediately executes the receiver shut-down sequence. If the PCD5008 is executing the shut-down sequence when turned on (with the ON bit in the control packet set) the PCD5008 completes the shut-down sequence before starting the warm-up sequence.

8.5.8.1 Receiver shut-down setting packets (ID = 1A to 1BH)

SE: step enable (Table 21). The receiver setting is enabled when the bit is set. If the bit is cleared then that step in the receiver shut-down sequence is disabled and all following steps are ignored. Value after reset = 0.

LBC: low battery check (Table 21). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver shut-down state. Value after reset = 0.

CLS: control line setting (Table 21). This is the value to be output on the receiver control lines (S0 to S7) for this receiver shut-down state. Value after reset = 0.

ST: step time (Table 21). This sets the duration time for receiver shut-down, until the next receiver state. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01H) to 39.375 ms (ST = 3FH). Value after reset = 01H.

s: setting number, see Tables 20 and 21 for the s names and values and location in the receiver shut-down packet.

Table 20 s names and values

s	SETTING NAME
0	shut-down 1
1	shut-down 2

Table 21 Receiver shut-down stages

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	1	0	1	s
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

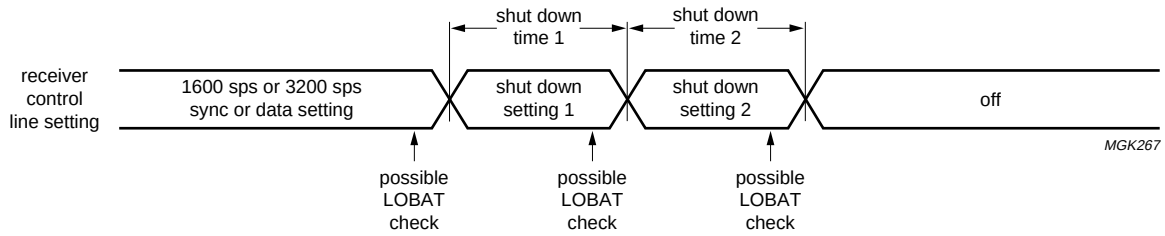


Fig.15 Receiver shut-down sequence.

8.6 Configuration of the FLEX™ CAPCODE

8.6.1 GENERAL

A CAPCODE specifies a decoder address, the collapse value of the address and whether single-phase, any-phase or all-phase address. The PCD5008 supports single-phase and any-phase operation. The FLEX™ protocol provides a standard mechanism to derive phase and frame in which an address should be transmitted. If this mechanism is not used, a CAPCODE also specifies the phase and frame assigned to the address.

8.6.2 CAPCODE FORMAT

The FLEX™ CAPCODE consist of a series of decimal and alphabetic fields, see Fig.16 for the field definitions.

When the FLEX™ standard pager collapse value of 4 (battery cycle of 16 frames) is used, the pager collapse field can be omitted.

The collapse value is a number between 0 and 7 and defines how often the decoding device looks for messages on the FLEX™ channel. For a given collapse value b, the decoding device looks in every 2^b frames. Thus an address with an assigned base frame of 3 and a collapse value of 5 typically looks for messages in frame 3 and every 32 frames thereafter (i.e. frames 3, 35, 67 and 99).

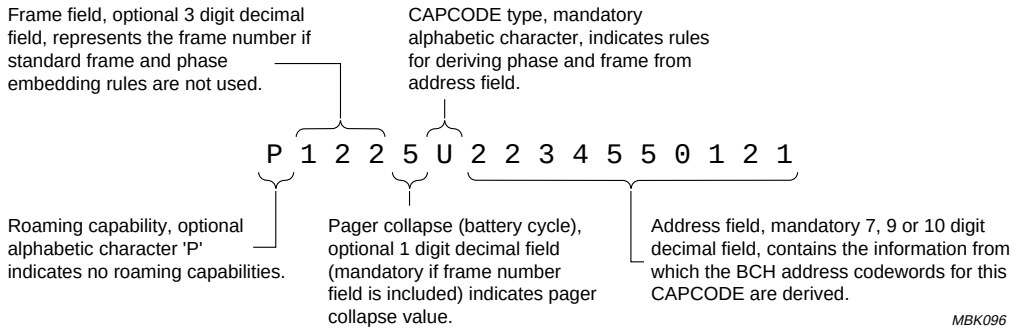


Fig.16 CAPCODE format.

8.6.3 CAPCODE RANGES

A CAPCODE represents user addresses ranging from 1 to 5370810366. A short CAPCODE can have address values below 2031615 and are represented in the data stream by a single address codeword. Some short addresses have been reserved for special purposes: information service addresses, network addresses, temporary (group) addresses and operator messaging addresses.

A long CAPCODE represents addresses situated above 2101248 subdivided into categories (uncoordinated, global, country) to allow different allocation schemes to coexist.

Table 22 defines the address usage assignment. All addresses not listed in this table are not defined and reserved for future use.

Table 22 CAPCODE assignment table

CAPCODE ADDRESS VALUE		DESCRIPTION
from	**to**	
0000000000		illegal
0000000001	0001933312	short addresses
0001933313	0001998848	illegal
0001998849	0002009087	reserved for future use
0002009088	0002025471	Information service addresses
0002025472	0002029567	network addresses
0002029568	0002029583	temporary addresses
0002029584	0002029599	operator messaging addresses
0002029600	0002031614	reserved for future use
0002031615	0002101248	invalid, not used
0002101249	0102101250	long address set 1-2 uncoordinated
0102101251	0402101250	long address set 1-2 country; note 1
0402101251	1075843072	long address set 1-2 global; note 2
1075843073	2149584896	long address set 1-3 global; note 2
2149584897	3223326720	long address set 1-4 global; note 2
3223326721	3923326750	long address set 2-3 country; note 1
3923326751	4280000000	long address set 2-3 reserved
4280000001	4285000000	long address set 2-3 information service, global; notes 2 and 3
4285000001	4290000000	long address set 2-3 information service, country; notes 1 and 3
4290000001	4291000000	long address set 2-3 information service, world-wide; notes 3 and 4
4291000001	4297068542	reserved for future use

Notes

1. Country: the addresses are coordinated within each country and with countries along borders.
2. Global: address is coordinated to be unique world-wide.
3. Information service: currently, the rules governing the use of these addresses are not defined.
4. World-wide: 1000 addresses are assigned to each country for world-wide use.

8.6.4 ADDRESS CALCULATION

Address codeword values generally do not coincide with (part of) the user address as specified in the CAPCODE. To find the address codewords corresponding to a user address a conversion has to be done (Table 24). The type of conversion depends on the CAPCODE range in which the user address is located. Note that addresses are transmitted LSB first (differently to POCSAG).

Short addresses, are transmitted in a single address codeword where as long addresses are transmitted in two consecutive address codewords. The first codeword of a long address contains the lower part of the address, the second codeword the upper part. By combining two long address codewords from different banks 6 long address ranges are created: 1 to 2, 1 to 3, 1 to 4, 2 to 3, 2 to 4 and 3 to 4. Ranges 2 to 4 and 3 to 4 are as yet undefined and reserved.

Table 24 describes how to calculate the 21 bit address codeword which is transmitted over the air.

Table 23 Address word range definitions

TYPE	HEX VALUE
Idle word (illegal address)	000000
Long address 1	000001 to 008000
Short address	008001 to 1E0000
Long address 3	1E0001 to 1E8000
Long address 4	1E8001 to 1F0000
Short address (reserved)	1F0001 to 1F27FF
Information service address	1F2800 to 1F67FF
Network address	1F6800 to 1F77FF
Temporary address	1F7800 to 1F780F
Operator messaging address	1F7810 to 1F781F
Short address (reserved)	1F7820 to 1F7FFE
Long address 2	1F7FFF to 1FFFFE
Idle word (illegal address)	1FFFFF

Table 24 Address word calculation

TYPE	LOWER ADDRESS CODEWORD; notes 1, 2 and 3	UPPER ADDRESS CODEWORD; notes 1, 3 and 4
Short address	CAPCODE + 8000	note 5
Long address, range 1 to 2; note 6	1 + ((CAPCODE – 1F9001) MOD 8000)	1FFFFF – ((CAPCODE – 1F9001) DIV 8000)
Long address, ranges 1 to 3 and 1 to 4	1 + ((CAPCODE – 1F9001) MOD 8000)	1D8000 + ((CAPCODE – 1F9001) DIV 8000)
Long address, range 2 to 3	1F7FFF + ((CAPCODE – 1F8FFF) MOD 8000)	1C8000 + ((CAPCODE – 1F8FFF) DIV 8000)

Notes

1. All numbers are in hexadecimal format.
2. The MOD operator gives the remainder of an integer division.
3. CAPCODE refers to the value of the address field in a FLEX™ CAPCODE.
4. The DIV operator is the integer division.
5. A short address consists of a single codeword.
6. The upper codeword range in bank 2 is used from the highest address downwards, i.e. the lowest value of the CAPCODE produces a codeword value of 1FFFFEH.

8.6.5 PHASE AND FRAME CALCULATION

The method for specifying the phase and base frame of a pager is specified in the CAPCODE type:

- The phase, base frame are extracted by standard rules from the user address field in the CAPCODE (CAPCODE types A to L).
- The phase is indicated by the CAPCODE type (Table 25) and the base frame is specified in the frame field of the CAPCODE (CAPCODE types U to Z).

For easy allocation of (up to 4) consecutive CAPCODEs having the same phase and frame, an offset in the range 0 to 3 is subtracted from the user address for the purposes of phase and frame extraction. The offset is determined by the CAPCODE type.

The standard rules for extracting phase and base frame from the user address are (phase numbers 0 to 3 correspond to phases A to D):

Phase number = ((Address – Offset) DIV 4) MOD 4

Frame = ((Address – Offset) DIV 16) MOD 128

where DIV is the integer division and MOD is the remainder of an integer division.

For a CAPCODE which does not use the standard rules for extracting phase and base frame (CAPCODE types U to Z) the 3-digit frame field 000 to 127 and a single digit decimal pager collapse 0 to 5 can precede the CAPCODE type. When these fields are not included, the paging device or the subscriber database must be accessed to determine the assigned frame and collapse value.

Table 25 Frame and phase extraction for different CAPCODE types

CAPCODE TYPE	PAGER TYPE	FRAME/PHASE EXTRACTION
A	single-phase	standard rules; Offset: 0
B	single-phase	standard rules; Offset: 1
C	single-phase	standard rules; Offset: 2
D	single-phase	standard rules; Offset: 3
E	any-phase	standard rules; Offset: 0
F	any-phase	standard rules; Offset: 1
G	any-phase	standard rules; Offset: 2
H	any-phase	standard rules; Offset: 3
I	all-phase; note 1	standard rules; Offset: 0
J	all-phase; note 1	standard rules; Offset: 1
K	all-phase; note 1	standard rules; Offset: 2
L	all-phase; note 1	standard rules; Offset: 3
U	single-phase	no frame extraction rules, phase-A
V	single-phase	no frame extraction rules, phase-B
W	single-phase	no frame extraction rules, phase-C
X	single-phase	no frame extraction rules, phase-D
Y	any-phase	no frame extraction rules, any-phase
Z	all-phase; note 1	no frame extraction rules, all-phase

Note

1. All-phase decoding is not defined in FLEX™ G1.8 and, therefore, is not supported by the PCD5008.

8.6.6 CONFIGURATION OF USER ADDRESSES (ID = 78H, 80H TO 8FH)

The PCD5008 has 16 user address locations which can be programmed as long or short, and configured as priority and/or tone-only. After a reset all address locations are disabled. Short addresses occupy a single location, long addresses occupy two locations. The first word of a long address must be in an even address location and the second word must be in the address index immediately following the first word. Address location containing long addresses of the 2-3 and 2-4 set (Section 8.6.3) must follow any address locations programmed as long addresses of the 1-2, 1-3 and 1-4 set.

User addresses are programmed using the address assignment packets, and are enabled and disabled using the address enable packet. To allow easy reprogramming of user addresses without disrupting normal operation, the host can send address assignment packets while the PCD5008 is on. In this case, the host must disable the user address location(s) by clearing the corresponding user address enable (UAE) bit in the UAE packet before changing any of the bits in the corresponding address assignment packet.

a: address location (Table 26). This specifies which address location is being configured. A zero in this field corresponds to address index zero (AI = 0) in the address packet received from the PCD5008 when an address is detected (Section 8.7.2).

LA: long address (Table 26). When this bit is set, the address is configured as a long address. Both words of a long address must have this bit set.

TOA: tone-only address (Table 26). When this bit is set, the PCD5008 considers this address a tone-only address and does not decode a vector word when the address is received. Both words of a long, tone only address must have this bit set.

A: address word (Table 26). This is the 21 bit value of the address word (A20 = MSB). Valid FLEX™ messaging addresses must be used. For the conversion from a CAPCODE (Section 8.6.4).

UAE: user address enable (Table 27). When a bit is set, the corresponding user address location is enabled. When it is cleared, the corresponding user address location is disabled. UAE_0 corresponds to the user address location configured using a packet ID of 80H and UAE_{15} corresponds to the user address location configured using a packet ID of 8FH. In some instances, if an invalid FLEX™ messaging address is programmed, it is not detected even when the address is enabled. Value after reset = 0.

Table 26 Address assignment packet bit assignments (ID = 80H to 8FH)

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	1	0	0	0	a_3	a_2	a_1	a_0
2	0	LA	TOA	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}
1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Table 27 Address enable packet bit assignments (ID = 78H)

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	0	0	0
2	0	0	0	0	0	0	0	0
1	UAE_{15}	UAE_{14}	UAE_{13}	UAE_{12}	UAE_{11}	UAE_{10}	UAE_9	UAE_8
0	UAE_7	UAE_6	UAE_5	UAE_4	UAE_3	UAE_2	UAE_1	UAE_0

8.6.7 CONFIGURATION OF ASSIGNED FRAMES AND PAGER COLLAPSE (ID = 20H TO 27H)

The assigned frame and collapse value determine the frames in which the decoding device typically looks for messages (other system factors can cause the decoding device to look in other frames in addition to the typical frames).

The PCD5008 must be configured explicitly to receive all required frames by setting the associated assigned frame (AF) bits. For each enabled CAPCODE these are the base frame and the associated frames implied by the pager collapse value. For example if the PCD5008 has one enabled address and it is assigned to base frame 3 with a collapse value of 4, the AF bits for frames 3, 19, 35, 51, 67, 83, 99 and 115 should be set and the AF bits for all other frames should be cleared. There are 8 frame assignment packets each capable of assigning a range of 16 consecutive frame numbers.

f: frame range, see Table 29 for location in the frame assignment packet and Table 28 for the AFs and values. The value determines which 16 frames out of a range of 128 correspond to the 16 AF bits in the packet. At least one of these bits must have been set when the PCD5008 is turned on by setting the ON bit in the control packet. Value after reset = 0.

AF: assigned frame (Table 29). If a bit is set, the PCD5008 decodes the associated FLEX™ frame and scans its contents for enabled addresses. Value after reset = 0.

Table 28 Frame assignment ranges

f_2	f_1	f_0	AF_{15}	AF_0
0	0	0	frame 127	frame 112
0	0	1	frame 111	frame 96
0	1	0	frame 95	frame 80
0	1	1	frame 79	frame 64
1	0	0	frame 63	frame 48
1	0	1	frame 47	frame 32
1	1	0	frame 31	frame 16
1	1	1	frame 15	frame 0

8.6.8 CONFIGURATION OF ASSIGNED PHASE

The assigned phase is required only for single-phase devices. It determines the phase (A, B, C, or D) in which the messages are received. For details of phase calculation see Section 8.6.5. For details of programming the assigned phase see Section 8.4.7.

Table 29 Frame assignment packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	1	0	0	f_2	f_1	f_0
2	0	0	0	0	0	0	0	0
1	AF_{15}	AF_{14}	AF_{13}	AF_{12}	AF_{11}	AF_{10}	AF_9	AF_8
0	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0

8.7 Call data packets

8.7.1 General

The PCD5008 sends data extracted from the FLEX™ signal to the host in SPI packets using the following packet types:

- BIW packets which contain data transmitted in BIWs
- Address packets which indicate that a call has been detected and give additional information about call attributes
- Vector packets which indicate the call type and indicate which message word numbers (WN) are associated with the call
- Message packets which contain the information contained within the message codewords of a call.

For more information about the function of these packets within the FLEX™ datastream see Section 8.8.

8.7.2 Address packet (ID = 01H)

Information from address codewords in received calls is sent to the host in address packets. If less than 3 bit errors are detected in a received address word and it matches an enabled address assigned to the PCD5008, the address packet is sent to the host processor. The address packet contains the call address, the location in the datastream of the associated vector, and other miscellaneous call data.

PA: priority address (Table 30). This bit is set if the address was received as a priority address.

p: phase (Table 30). This is the phase on which the address was detected (0 = A, 1 = B, 2 = C and 3 = D).

LA: long address (Table 30). This bit is set if the address was programmed in the PCD5008 as a LA.

AI: address index (Table 30). This index identifies which address was detected. Valid values are 00H to 0FH, corresponding to the 16 programmable address words and 80H to 8FH, corresponding to the 16 temporary addresses (Section 8.8.4). For long addresses, the address packet is only sent once with AI referring to the second word of the address.

TOA: tone-only address (Table 30). Set this bit if the address was programmed in the PCD5008 as a tone-only address. No vector word is sent for tone-only addresses.

WN: word number of vector (2 to 87 decimal) (Table 30). The location of the vector within this frame for the detected address. This value is invalid for this packet if the TOA bit is set.

x: unused bits (Table 30). The value of these bits is not guaranteed.

8.7.3 Vector packets (ID = 02H to 57H)

Information from vector codewords in received calls is sent to the host in vector packets. For any address packet sent to the host (except tone-only addresses), a corresponding vector packet is always sent.

The ID of the vector packet is the word number where the vector word was received in the frame. The host must associate vector packets with a call by searching for an address packet previously received on the same phase and with WN bits which match the ID of the vector packet.

The vector type of a vector packet indicates the format of a call as one of:

- Numeric (3 types)
- Short message/tone-only
- Hex/binary
- Alphanumeric
- Secure message
- Short instruction.

The numeric, hex/binary, alphanumeric, and secure message vector packets indicate the location and number of message word packets in the message field. If more than two bit errors are detected in the vector word (via BCH calculations, parity calculations, check character calculations, or value validation) the e bit is set and the message words are not sent.

Table 30 Address packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	1
2	PA	p_1	p_0	LA	x	x	x	x
1	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0
0	TOA	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0

8.7.4 NUMERIC VECTOR PACKET

WN: word number of vector (2 to 87 decimal) (Table 31). WN describes the location of the vector word in the frame.

e: error (Table 31). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 31). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

K: first check bits of the message checksum (Table 31 and Section 8.8.6).

n: number of message words in the message (Table 31), including the second vector word for long addresses, (000 = 1 word message, 001 = 2 word message, etc.). For long addresses, the first message word is located in the word location that immediately follows the associated vector.

b: word number of message start in the message field (3 to 87 decimal) (Table 31). For long addresses, the word number indicates the location of the second message word.

x: unused bits (Table 31). The value of these bits is not guaranteed.

V: vector type identifier (Table 32).

Table 31 Numeric vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	K_3	K_2	K_1	K_0	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

Table 32 Numeric vector definitions

V_2	V_1	V_0	TYPE	DESCRIPTION
0	1	1	standard numeric	No special formatting of characters is specified.
1	0	0	special format numeric	Formatting of the received characters is predetermined by special rules in the host (e.g. inserting spaces and dashes).
1	1	1	numbered numeric	Received information is numbered by the service provider to indicate all messages have been properly received.

8.7.5 SHORT MESSAGE/TONE-ONLY VECTOR PACKET

V: vector type identifier, these bits set to 010 for a short message/tone-only vector (Table 33).

WN: word number of vector (2 to 87 decimal) (Table 33). WN describes the location of the vector word in the frame.

e: error (Table 33). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 33). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

t: message type (Tables 33 and 34). These bits define the meaning of the d bits in this packet.

x: unused bits (Table 33). The value of these bits is not guaranteed.

d: data bits whose definition depends on the value of t in this packet according to Table 34. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder sends a message packet from the word location immediately following the vector packet. Except for the short message on a non-network address (t = 0), all messages bits in the message packet are unused and should be ignored.

Table 33 Short message/tone-only vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{11}	d_{10}	d_9	d_8	d_7	d_6
0	d_5	d_4	d_3	d_2	d_1	d_0	t_1	t_0

Table 34 Short message/tone-only vector definitions

t_1	t_0	d_{11}	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	DESCRIPTION
0	0	c_3	c_2	c_1	c_0	b_3	b_2	b_1	b_0	a_3	a_2	a_1	a_0	first 3 numeric characters; note 1
0	1	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	S_2	S_1	S_0	8 sources (S) and 9 unused bits (s)
1	0	s_1	s_0	R_0	N_5	N_4	N_3	N_2	N_1	N_0	S_2	S_1	S_0	8 sources (S), message retrieval flag (R), message number (N) and 2 unused bits (s)
1	1													spare message type

Note

1. For long addresses, an extra 5 characters are sent in the message packet immediately following the vector packet.

8.7.6 HEX/BINARY, ALPHANUMERIC AND SECURE MESSAGE VECTORS

V: vector type identifier (Table 35).

WN: word number of vector (2 to 87 decimal) (Table 36). WN describes the location of the vector word in the frame.

e: error (Table 36). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 36). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

n: number of message words in this frame (Table 36), including the first message word that immediately follows a long address vector. Valid values are 1 to 85 decimal.

b: word number of message start in the message field (Table 36). Valid values are 3 to 87 decimal.

x: unused bits (Table 36). The value of these bits is not guaranteed.

Note that for long addresses, the first message packet is sent from the word location immediately following the word location of the vector packet. The b bits indicate the second message word in the message field if one exists.

Table 35 Non-numeric vector definitions

V_2	V_1	V_0	TYPE
0	0	0	secure
1	0	1	alphanumeric
1	1	0	hex/binary

Table 36 Hex/binary, alphanumeric and secure message vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	n_6	n_5	n_4	n_3	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

8.7.7 SHORT INSTRUCTION VECTOR

V: these bits are set 001 for a short instruction vector.

WN: word number of vector (2 to 87 decimal) (Table 37). WN describes the location of the vector word in the frame.

e: error (Table 37). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 37). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

i: instruction type (Tables 37 and 38). These bits define the meaning of the d bits in this packet.

x: unused bits (Table 37). The value of these bits is not guaranteed.

d: data bits whose definition depend on the value of the i bits in this packet according to Table 38. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder sends a message packet immediately following the vector packet. All message bits in the message packet are unused and should be ignored.

Table 37 Short instruction vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{10}	d_9	d_8	d_7	d_6	d_5
0	d_4	d_3	d_2	d_1	d_0	i_2	i_1	i_0

Table 38 Short instruction vector definitions

i_2	i_1	i_0	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	DESCRIPTION
0	0	0	a_3	a_2	a_1	a_0	f_6	f_5	f_4	f_3	f_2	f_1	f_0	temporary address assignment, note 1
0	0	1												reserved
0	1	0												reserved
0	1	1												reserved
1	0	0												reserved
1	0	1												reserved
1	1	0												reserved
1	1	1												reserved for test

Note

1. Assigned temporary address index a and associated frame number f (Section 8.8.4).

8.7.8 MESSAGE PACKETS (ID = 03H TO 57H)

8.7.8.1 General

The message field follows the vector field in the FLEX™ protocol. It contains the message data, checksum information, and may contain fragment and message numbers (Sections 8.8.7 and 8.8.5). If the error bit of a vector word is not set and the vector word indicates that there are message words associated with the page, the message words are sent in message packets to the host.

The ID of the message packet is the word number where the message word was received in the frame.

WN: word number of message word (3 to 87 decimal) (Table 40). WN describes the location of the message word in the frame.

e: error (Table 40). Set if more than 2 bit errors are detected in the word.

p: phase (Table 40). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

i: these are the information bits of the message word (Table 40). The definition of these i bits depends on the vector type and which word of the message is being received.

8.7.8.2 Numeric Message

FLEX™ numeric messages are encoded using the 4-bit BCD encoded characters sets described in Table 39. Characters are placed in codewords along with additional information about the message as described in Tables 41 and 42 and the following definitions. The 4-bit numeric characters of the message are designated as letters a, b, c, d, ... z, A, B etc.

Only codewords containing the numeric message are to be transmitted. The space character CH is used to fill any unused 4-bit characters in the last word and zeros to fill any remaining partial characters. The checksum includes only the codewords comprising the shortened message, along with the space and fill characters used to fill in the last word.

Table 39 Standard and alternate numeric character sets; Peoples Republic of China (ROC) option ‘on’ and ‘off’

B_3	B_2	B_1	B_0	CHARACTER	
				ROC ‘on’	ROC ‘off’
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	Spare
1	0	1	1	B	U
1	1	0	0	Space	Space
1	1	0	1	C	–
1	1	1	0	D	]
1	1	1	1	E	[

Table 40 Message packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	i_{20}	i_{19}	i_{18}	i_{17}	i_{16}
1	i_{15}	i_{14}	i_{13}	i_{12}	i_{11}	i_{10}	i_9	i_8
0	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0

K: least significant 2 bits of 6 bit message checksum (Tables 41 and 42), most significant 4 bits are in the vector word. See Section 8.8.6 for a description of message checksums.

N: message number (Table 42). See Section 8.8.7 for a description of message numbering.

R: message retrieval flag (Table 42). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

S: special format, (Table 42). In the numbered message format, when this bit is set, a special display format should be used. Spaces and dashes, specified by the host, are inserted into the received message to ease reading of the message. This feature may avoid the transmission of an additional word on the channel. The actual format is undefined in FLEX™ and may be determined by the manufacturer.

Table 41 Standard (V = 011) or special format (V = 100) 4, 10, 15, 20, 25, 31, 36, or 41 characters

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2
2nd	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3
3rd	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0
4th	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1
5th	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2
6th	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3
7th	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0
8th	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	T_0	T_1	T_2	T_3	U_0	U_1

Table 42 Numbered (V = 111) 2, 8, 13, 18, 23, 29, 34, or 39 numeric characters

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	N_0	N_1	N_2	N_3	N_4	N_5	R_0	S_0	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2
2nd	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3
3rd	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0
4th	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1
5th	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2
6th	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3
7th	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0
8th	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1

8.7.8.3 Alphanumeric Message

FLEX™ alphanumeric messages are encoded using the 7-bit encoded alphanumeric character set defined in Table 43. Characters are placed in codewords along with additional information about the message as described in Tables 44 and 45 and the following definitions. The 7-bit characters of the message are designated lower case letters a, b, c, d, etc.

Alphanumeric messages can be sent as fragments. See Section 8.8.5 for a description of message fragmentation.

Control characters that are not acted upon by the pager are ignored in the display process (do not require display space) but are stored in memory for possible download to an external device. The ASCII character ETX (03H) should be used to fill any unused 7-bit characters in a word.

Where symbolic characters (e.g. Chinese, Kanji etc.) are being transmitted, special rules for fragment and message termination are defined in Section 8.8.5.1.

Each 7-bit field, starting with the second character of the second word in the message (first character of the second word in all remaining fragments), represents standard ASCII (ISO 646-1983E) characters with options for certain international characters.

Table 43 FLEX™ alphanumeric character set

LEAST SIGNIFICANT 4 BITS OF CHARACTER (HEX)	MOST SIGNIFICANT 3 BITS OF CHARACTER (HEX)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	NUL	DLE	SP	0	@	P	‘	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	“	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	’	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	TAB	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

K: 10-bit fragment checksum (Tables 44 and 45). See Section 8.8.6 for a description of message checksum.

C: 1-bit message continued flag (Tables 44 and 45). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2-bit message fragment number (Tables 44 and 45). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Tables 44 and 45). See Section 8.8.7 for a description of message numbering.

M: 1-bit mail drop flag (Table 44). When this bit is set, it indicates the message is to be stored in a special area in memory and is written over existing data automatically in that memory space.

R: message retrieval flag (Table 44). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

S: 7-bit signature field (Table 44). The signature is defined to be the 1's complement of the binary sum over the total message (all fragments). 7 bits at a time are taken (on alpha character boundary) starting with the first 7 bits directly following the signature field, $a_6a_5a_4a_3a_2a_1a_0$, $b_6b_5b_4b_3b_2b_1b_0$, etc. The 7 LSBs of the result are transmitted as the message signature.

U, V: fragmentation control bits (Table 45). This field exists in all fragments except the first fragment. It is used to support character position tracking in each fragment when symbolic characters (character made up of 1, 2 or 3 ASCII characters) are transmitted using the alphanumeric message type. The default value is 0,0. See Section 8.8.5.1 for a description of fragment control.

Table 44 Vector type V = 101 first fragment

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	R_0	M_0
2nd	S_0	S_1	S_2	S_3	S_4	S_5	S_6	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6
3rd	c_0	c_1	c_2	c_3	c_4	c_5	c_6	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6
4th	f_0	f_1	f_2	f_3	f_4	f_5	f_6	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6
5th	i_0	i_1	i_2	i_3	i_4	i_5	i_6	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 45 Vector type V = 101 other fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	U_0	V_0
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

8.7.8.4 Hex/binary message

FLEX™ hexadecimal/binary messages may be encoded using any word size (blocking length) in the range 1 to 16 bits. Words are placed in codewords along with additional information about the message as described in Tables 46 and 47 and these definitions. The message data in Tables 46 and 47 have blocking lengths of 4 bits; words are designated lower case letters a, b, c, d etc.

Hexadecimal/binary messages can be sent as fragments. See Section 8.8.5 for a description of message fragmentation. Messages and message fragments are terminated, or interrupted in the case of a non-terminating fragment, on the last full character boundary in the last codeword. Unused bits are cleared if the last valid data bit is logic 1, or set if the last valid data bit is logic 0. If the terminating fragment exactly fills its last codeword, an additional codeword is sent to indicate the location of the last character. This codeword is filled with logic 0s if the last valid data bit is logic 1 and filled with logic 1s if the last valid data bit is logic 0.

Fields K to N make up the first word of a message and the first word of every fragment in a long message.

K: 12 bit fragment checksum (Tables 46 and 47). See Section 8.8.6 for a description of message checksums.

C: 1 bit message continued flag (Tables 46 and 47). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2 bit message fragment number (Tables 46 and 47). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Tables 46 and 47). See Section 8.8.7 for a description of message numbering.

H: 1 bit header message flag (Table 46). It is a header message only when this bit is set, otherwise it is a data message. A header message is a displayable tag associated with a non-displayable data message. The header message (which is sent first) and the data message, both have the same message number.

The second codeword of the first fragment of a hex/binary message contains fields R to S. These fields are only transmitted in the first fragment of a message.

R: message retrieval flag (Table 46). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

s: 5 bit field reserved for future use (Table 46). Default value = 00000.

M: 1 bit mail drop flag, see Table 46. When this bit is set, the message is to be stored in a special area in memory to overwrite existing data in the same memory space.

D: 1 bit display direction field (Table 46). D = 0 display left to right, D = 1 display right to left (valid only when data sent as characters i.e. blocking length not equal 0001).

B: 4 bit blocking length (Table 46). Indicates bits per character. $B_3B_2B_1B_0$ = 0001 = 1 bit per character (binary/transparent data), 1111 = 15 bits per character, 0000 = 16 bits per character. Data with a blocking length other than 1 is assumed to be displayed on a character by character basis (default value = 0001). Note: Tables 46 and 47 show B = 4 bit blocking length.

S: 8 bit signature field (Table 46). The 1's complement of the binary sum, taken 8 bits at a time, over the total message prior to formatting into fragments. The first 8 bits following the signature field are summed with the following 8 bits, $b_3b_2b_1b_0a_3a_2a_1a_0 + d_3d_2d_1d_0c_3c_2c_1c_0$, etc. continuing to the last valid data bit in the last word of the last fragment (the sum does not include termination bits). The 8 LSBs of the result are inverted (1's complement) and transmitted as the message signature.

8.7.8.5 Secure message

FLEX™ secure messages are encoded using the 7-bit FLEX™ alphanumeric character set (Section 8.7.8.3). These characters are placed in codewords along with additional information about the message as described in Table 48 and the following definitions. In Table 48, 7-bit characters of the message are designated lower case letters a, b, c, d etc.

Secure messages follow the same fragmentation and termination rules as alphanumeric messages (Section 8.7.8.3).

K: 10 bit fragment checksum (Table 48). See Section 8.8.6 for a description of message checksums.

C: 1 bit message continued flag (Table 48). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2 bit message fragment number (Table 48). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Table 48). See Section 8.8.7 for a description of message numbering.

s: spare bits (Table 48), are not used and are set to 0.

Table 46 Vector type V = 110 first fragment

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	R_0	M_0	D_0	H_0	B_0	B_1	B_2	B_3	s_0	s_1	s_2	s_3	s_4	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
3rd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
4th	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
5th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
6th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 47 Vector type V = 110 all other fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
3rd	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
4th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
5th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 48 Vector type V = 000 all fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	s_0	s_1
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

8.7.9 BLOCK INFORMATION WORD (BIW) PACKET (ID = 00H)

The FLEX™ protocol allows systems to transmit time information using block information words. The information carried in a BIW depends on the BIW word format (Table 49). The first BIW of each phase, carrying information about the frame structure, is used internally by the PCD5008 and is never transmitted to the host.

The PCD5008 can be configured to send all time and date BIWs (BIW001, BIW010 and BIW101) to the host by setting the SBI bit in the control packet, see Section 8.4.7. When the SBI bit is set and a BIW is received with an uncorrectable number of bit errors, the PCD5008 sends the BIW to the host indicating that the codeword was received in error (regardless of the BIW word format). The PCD5008 does not support decoding of vector and message words associated with the data/system message BIW101.

System providers supporting local time transmissions are required to transmit at least one time related BIW in each phase transmitted in frame 0, cycle 0. The time transmitted is the local time for the transmitted time zone and refers to the actual time at the leading edge of the first bit of sync 1 of frame 0 of the current cycle.
See Tables 50, 51, 52 and 53 and the following bit definitions of the time related BIWs.

e: error (Table 49). Set if more than 2 bit errors are detected in the word or if the check character calculation fails after error correction has been performed.

p: phase (Table 49), is the phase on which the BIW was found (0 = A, 1 = B, 2 = C and 3 = D).

x: unused bits (Table 49). Their value is not guaranteed.

f: word format type (Table 49). The value of these bits modify the meaning of the s bits in this packet as described in Tables 50, 51 and 52. If the e bit is not set, this field is one of 001, 010 or 101.

s: BIW information bits (Table 49). The definition of these bits depend on the f bits in this packet.

m: month field (Table 50). 0001 to 1100 binary correspond to January to December in month order.

d: day field (Table 50). 00001 to 11111 binary correspond to 1 to 31 days in the month.

Table 49 BIW packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	0
2	e	p_1	p_0	x	x	f_2	f_1	f_0
1	x	x	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8
0	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

Table 50 Month/day/year BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0
0	0	1	m_3	m_2	m_1	m_0	d_4	d_3	d_2	d_1	d_0	Y_4	Y_3	Y_2	Y_1	Y_0

Table 51 Second/minute/hour BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0
0	1	1	S_2	S_1	S_0	M_5	M_4	M_3	M_2	M_1	M_0	H_4	H_3	H_2	H_1	H_0

Table 52 Accurate seconds/daylight savings time/time zone; system message BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	DESCRIPTION
1	0	1	S_2	S_1	S_0	x	L_0	z_4	z_3	z_2	z_1	z_0	0	1	0	X	system message; note 1

Note

1. When the $s_3s_2s_1s_0$ field is 0100 or 0101, then s_4 to s_{13} are defined as above, when the $s_3s_2s_1s_0$ field does not have one of these values, the system message does not contain time related information and is not sent to the host.

Y: year field (Table 50). This represents the year with modulo 32 arithmetic. 00000 to 11111 binary representing years 1994 to 2025 and 2026 to 2057.

S: seconds field (Table 51). This represents a coarse value of the seconds field. These bits represent the seconds in $\frac{1}{8}$ minute (7.5 s) increments.
000 to 111 binary correspond to 0 to 52.5 seconds.

M: minute field (Table 51). 000000 to 111011 binary correspond to 0 to 59 minutes.

H: hour field (Table 51). 00000 to 10111 binary correspond to 0 to 23 hours.

S: accurate seconds (Table 52). This field provides a more accurate seconds reference and can be used to adjust the seconds to within 1 second. This field represents the time that should be added to the coarse seconds in $\frac{1}{64}$ minute increments.

L: daylight savings time (Table 52). When this bit is set, the time being transmitted is local standard time. When it is clear, the time being transmitted is daylight savings time.

z: time zone (Table 52). These bits indicate the time zone for the time which is being transmitted. The offset from GMT is the offset for local standard time. Table 53 describes the values for **z**.

Table 53 Time zone values

z_4	z_3	z_2	z_1	z_0	TIME ZONE
0	0	0	0	0	GMT
0	0	0	0	1	GMT + 01:00h
0	0	0	1	0	GMT + 02:00h
0	0	0	1	1	GMT + 03:00h
0	0	1	0	0	GMT + 04:00h
0	0	1	0	1	GMT + 05:00h
0	0	1	1	0	GMT + 06:00h
0	0	1	1	1	GMT + 07:00h
0	1	0	0	0	GMT + 08:00h
0	1	0	0	1	GMT + 09:00h
0	1	0	1	0	GMT + 10:00h
0	1	0	1	1	GMT + 11:00h
0	1	1	0	0	GMT + 12:00h
0	1	1	0	1	GMT + 03:30h
0	1	1	1	0	GMT + 04:30h
0	1	1	1	1	GMT + 05:30h

z_4	z_3	z_2	z_1	z_0	TIME ZONE
1	0	0	0	0	reserved
1	0	0	0	1	GMT + 05:45h
1	0	0	1	0	GMT + 06:30h
1	0	0	1	1	GMT + 09:30h
1	0	1	0	0	GMT – 03:30h
1	0	1	0	1	GMT – 11:00h
1	0	1	1	0	GMT – 10:00h
1	0	1	1	1	GMT – 09:00h
1	1	0	0	0	GMT – 08:00h
1	1	0	0	1	GMT – 07:00h
1	1	0	1	0	GMT – 06:00h
1	1	0	1	1	GMT – 05:00h
1	1	1	0	0	GMT – 04:00h
1	1	1	0	1	GMT – 03:00h
1	1	1	1	0	GMT – 02:00h
1	1	1	1	1	GMT – 01:00h

8.8 Message reception

8.8.1 FLEX™ SIGNAL STRUCTURE

The FLEX™ signal transmitted on the radio channel (see Fig.17) consists of a series of four minute cycles, each cycle having 128 frames at 1.875 seconds per frame. A pager may be assigned to process any number of the frames. Battery saving is performed for frames which are not assigned. The FLEX™ signal can assign additional frames to the pager using collapse, fragmentation, temporary addressing or carry-on information within the FLEX™ signal.

Each FLEX™ frame has a synchronization portion followed by an eleven block data portion, each block lasting 160 milliseconds. The synchronization portion indicates the rate at which the data portion is transmitted, 1600, 3200 or 6400 bits per second (bps). The 1600 bps rate is transmitted at 1600 symbols per second (sps) using 2 level FSK modulation and consists of a single phase of information at 1600 bps, phase-A. The 3200 bps rate is transmitted at either 1600 sps using 4 level FSK modulation or 3200 sps using 2 level FSK modulation and consists of two concurrent phases of information at 1600 bps, phase-A and phase-C. The 6400 bps rate is transmitted at 3200 sps using 4 level FSK modulation and consists of four concurrent phases of information at 1600 bps (phase-A, -B, -C and -D).

Each block has eight interleaved words per phase, thus there are 88 codewords (numbered 0 to 87) per phase in every frame. Each word has information contained within an error correcting code which allows for bit error correction and detection. The 88 words in each phase are organized into a block information field, an address field, a vector field, a message field, and an idle field. The boundaries between the fields are independent of the block boundaries. Furthermore, at 3200 and 6400 bps, the information in one phase is independent of the information in a concurrent phase, and the boundaries between the fields of one phase are unrelated to the boundaries between the fields in a concurrent phase.

The synchronization portion consists of: a first sync signal at 1600 bps; a frame information word having the frame number 0 to 127 (7 bits) and the cycle number 0 to 14 (4 bits); and a second sync signal at the data rate of the interleaved portion.

The block information field contains BIWs. These can be used for determining time and date information and certain paging system information.

The address field contains addresses assigned to paging devices. Addresses are used to identify information sent to individual paging devices and/or groups of paging devices. Information in the FLEX™ signal may indicate that an address is a priority address. An address may be either a short (one word) address or a long (two word) address. An address may be a tone-only address in which case there is no additional information associated with the address. If an address is not a tone-only address, then there is an associated vector word in the vector field. Information in the FLEX™ signal indicates the location of the vector word in the vector field associated with the address. A pager may perform battery saving at the end of the address field when its address(es) is not detected.

The vector field consists of a series of vector words. Depending upon the type of message, a vector word (or words in the case of a long address) may either contain all of the information necessary for the message, or indicate the location of message words in the message field comprising the message information. Short addresses have one associated vector word in the vector field. Long addresses have one associated vector word in the vector field directly followed by the first message codeword of the call.

The message field consists of a series of information words containing message information. The message information may be formatted in ASCII, BCD or binary depending upon the message type.

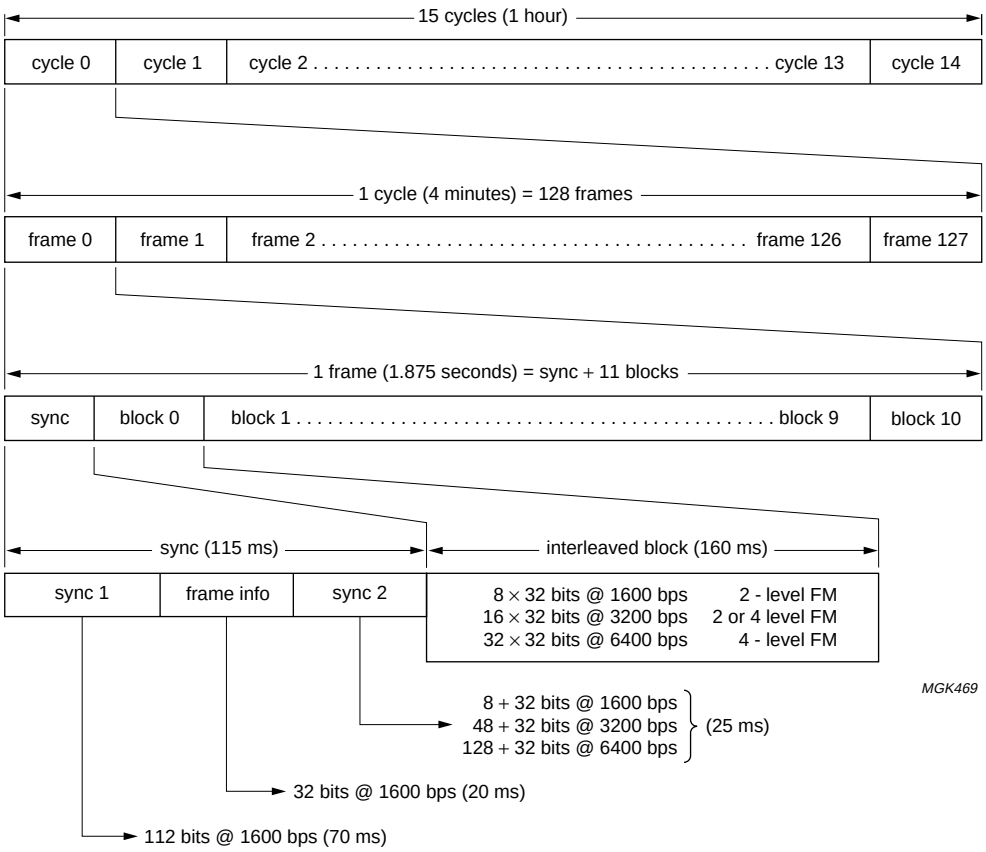


Fig.17 FLEX™ signal structure.

8.8.2 MESSAGE BUILDING

The PCD5008 sends data from the FLEX™ signal to the host in packets. Data is transmitted one block at a time, and one phase at a time. For a 2 phase transmission, information in block 0 phase-A is converted into packets and sent to the host, then information in block 0 phase-C is sent to the host followed by information in block 1 phase-A and then information in block 1 phase-C etc. Codewords for different calls may therefore be interleaved, so the host must use the phase and word number embedded in each packet to associate that packet with a particular call.

The phase and word number of the vector packet provides a unique key which allows the host to associate all the data for a particular call within a frame. The host must then use information embedded in the vector word to calculate what message word locations are associated with the vector.

Table 54 FLEX™ transmission sequence

BLOCK	WORD	PHASE-A	PHASE-C
0	0	BIW1; note 1	BIW1; note 1
	1	addr; note 2	BIW
	2	addr; note 2	BIW
	3	$addr_1$	addr; note 2
	4	$addr_2$	addr; note 2
	5	vect; note 2	long $addr_3$ (cw 1)
	6	vect; note 2	long $addr_3$ (cw 2)
	7	$vect_1$	addr; note 2
1	8	$vect_2$	vect; note 2
	9	$mess_1$ (cw 1)	vect; note 2
	10	$mess_1$ (cw 2)	$vect_3$; note 3
	11	$mess_1$ (cw 3)	$mess_3$ (cw 1); note 4
	12	$mess_2$ (cw 1)	mess; note 2
	13	$mess_2$ (cw 2)	mess; note 2
	14	$mess_2$ (cw 3)	$mess_3$ (cw 2)
	15	$mess_2$ (cw 4)	$mess_3$ (cw 3)

Notes

1. Phases begin with BIW1, which is not sent to the host.
2. Codewords not addressed to the pager.
3. Vector for long address indicates the location of the second and third message words.
4. For long addresses, the first message word immediately follows the vector.

Tables 54 and 55 show an example of receiving three messages (possibly portions of fragmented or group messages), and two BIW packets in the first two blocks of a 2 phase 3200 bps FLEX™ frame in case of an any-phase pager. Table 54 shows the block number, word number and word content of both phase-A and phase-C (subscripts indicate the call number). In a 6400 bps FLEX™ frame, there would be four phases: A, B, C and D; in a 1600 bps signal there would be only phase-A. Table 55 shows the sequence of packets transmitted to the host.

Table 55 PCD5008 packet sequence

PACKET	PHASE	PACKET TYPE	WORD NO.	COMMENT
1	A	address	7	note 1
2	A	address	8	note 1
3	A	vector	7	pointer to phase-A word 9
4	C	BIW	n.a.	note 2
5	C	BIW	n.a.	note 2
6	C	long address	10	note 1
7	A	vector	8	pointer to phase-A word 12
8	A	message	9	$mess_1$ (cw 1)
9	A	message	10	$mess_1$ (cw 2)
10	A	message	11	$mess_1$ (cw 3)
11	A	message	12	$mess_2$ (cw 1)
12	A	message	13	$mess_2$ (cw 2)
13	A	message	14	$mess_2$ (cw 3)
14	A	message	15	$mess_2$ (cw 4)
15	C	vector	10	pointer to phase-A word 14
16	C	message	11	$mess_3$ (cw 1)
17	C	message	14	$mess_3$ (cw 2)
18	C	message	15	$mess_3$ (cw 3)

Notes

1. Word number in an address is that of the corresponding vector.
2. BIW sent if BIW reception enabled by SBI bit in the control packet.

8.8.3 ALL FRAME MODE (ID = 03H)

The FLEX™ protocol requires pagers to be capable of receiving data in frames other than pagers' programmed frames and frames implied by collapse values. This is achieved in the PCD5008 by all frame mode (AFM) which is required to implement the following features:

- Fragmented messages Section 8.8.5)
- Temporary addresses (Section 8.8.4).

The PCD5008 enters AFM automatically and when in AFM, it decodes every FLEX™ frame irrespective of whether it is a programmed frame. In AFM the PCD5008 sends a status packet with the end-of-frame (EOF) bit set at the end of every frame. In addition the host can force AFM by sending an AFM packet with the force all frame mode (FAF) bit set.

The PCD5008 contains a number of counters which are used to track the number of active calls requiring AFM. These consist of an AFM counter for tracking the number of active fragmented messages and 16 temporary address enable (TAE) counters which count the number of times each temporary address has been enabled. These counters are automatically incremented when a corresponding vector is received, i.e.:

- A short instruction vector indicating a temporary address has been assigned to this pager
- A vector indicating a message for this pager with a format which allows fragmentation.

The host must determine when no further data can be received for a message associated with a temporary address, or a fragmented message, and send an AFM packet, see Table 56, to decrement the appropriate counter. AFM remains active until the host determines that no further data can be sent to it outside programmed frames, i.e:

- The TAE counters are all zero indicating that no further temporary message data is expected
- The AFM counter is zero indicating that no further data is expected for fragmented messages
- The FAF bit is clear.

Both the AFM counter and the TAE counters can only be incremented internally by the PCD5008 and can only be decremented by the host via AFM packet. Neither the TAE counters nor the AFM counter can be incremented past the value 127 (it does not roll-over) or decremented past the value 0. The TAE counters and the AFM counter are cleared on a reset and when the decoder is turned off.

DAF: decrement all frame mode counter, see Table 56. Setting this bit decrements the AFM counter by one. If a packet is sent with this bit clear, the AFM counter is not affected. Value after reset = 0.

FAF: force all frame mode, see Table 56. Setting this bit forces the PCD5008 to enter AFM. If this bit is clear, the PCD5008 may or may not be in AFM depending on the status of the AFM counter and the TAE counters. This functionality may be useful in acquiring transmitted time information. Value after reset = 0.

DTA: decrement temporary address enable counter, see Table 56. When a bit in this word is set, the corresponding TAE counter is decremented by one. When a bit is clear, the corresponding TAE counter is not affected. When a TAE counter reaches zero, the temporary address is disabled. Value after reset = 0.

Table 56 All frame mode packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	1	1
2	DAF	FAF	0	0	0	0	0	0
1	DTA_{15}	DTA_{14}	DTA_{13}	DTA_{12}	DTA_{11}	DTA_{10}	DTA_9	DTA_8
0	DTA_7	DTA_6	DTA_5	DTA_4	DTA_3	DTA_2	DTA_1	DTA_0

8.8.4 TEMPORARY ADDRESSES

FLEX™ allows dynamic group calls in which a common message is sent to a group of paging devices. This is achieved by assigning the same temporary address (TA) to each pager in the group using the pagers' personal addresses and the short instruction vector. The short instruction vector causes the TA to be active in the next occurrence of a specific frame (if the designated frame is equal to the present frame the host is to interpret this as the next occurrence of this frame in the following cycle).

FLEX™ specifies sixteen TAs which remain valid for one message starting in the specified frame and remaining valid throughout the following frames to the completion of the message. The FLEX™ protocol restricts the placement of TAs such that once assigned to a specific frame they cannot occur in the FLEX™ transmission before that frame.

The PCD5008 uses AFM (Section 8.8.3) to allow the reception of TAs outside programmed frames.
The sequence for the host and the PCD5008 to operate a TA is:

1. The PCD5008 receives an address codeword followed by a vector codeword with $V_2V_1V_0 = 001$ and $I_2I_1I_0 = 000$ indicating a short instruction vector which assigns a TA to this pager.
2. The PCD5008 passes the address and vector codeword to the host as packets and increments the corresponding TA counter and enters AFM.
3. The host examines the vector packet to identify which TA is assigned and the frame in which the TA is expected.
4. The PCD5008 continues to decode all of the frames and passes any address information, vector information and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
5. The host processes data packets received while the PCD5008 is in AFM. It uses the AFM packet to decrement the appropriate TA counter when no further data can be expected for the corresponding TA. This occurs when:
   a) The TA is not found in the assigned frame.
   b) The TA is found in the frame it was assigned and was not a fragmented message.
   c) The TA is found in the assigned frame was a fragmented message and the rules for message fragmentation (Section 8.8.5) indicate that no further data can be expected. In this case the host must send an AFM packet with both the DAF and the appropriate DTA bits set in order to terminate both the fragmented message and the TA.
6. The above operation is repeated for every enabled TA.

8.8.5 MESSAGE FRAGMENTATION

The FLEX™ frame length limits the maximum number of message codewords that can be associated with an address codeword. Messages longer than 84 codewords must be sent as several fragments. The PCD5008 uses AFM (Section 8.8.3) to allow the reception of fragmented messages.

The fragments of a message are sent in sequence. Each fragment contains a checksum character to detect errors in the fragment, a message number to identify which message the fragment is a part, and the continue bit which either indicates that more fragments are in queue or that the last fragment has been received. Each fragment also contains a fragment number starting with 3 for the first fragment and then incremented through the sequence 0, 1 or 2 in subsequent fragments. This allows the detection of missing fragments.

Message fragments may not be separated by more than 32 frames (1 minute) or 128 frames (4 minutes), as indicated by the service provider. During the reception of a fragmented message, the PCD5008 examines every frame for additional fragments until the last fragment is encountered or the host determines that more than 32 or 128 frames have elapsed since the reception of the previous message fragment.

The sequence for the host and the PCD5008 to receive a fragmented message is as follows:

1. The PCD5008 receives an address codeword followed by a vector indicating one of:
   a) Secure (vector type = 000)
   b) Alphanumeric (vector type = 101)
   c) Hexadecimal/binary (vector type = 110).

   The PCD5008 passes the address, vector and message codewords to the host as packets and increments its internal AFM counter and enters AFM.
2. While in AFM, the PCD5008 decodes all of the frames passing any address, vector and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
3. Every time the host receives a secure, alphanumeric or hexadecimal/binary vector packet, it inspects the message continued flag (C) in the first message packet:
   a) If this is not a fragmented message (C is clear and no fragmented messages are in progress for this address and message number), then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set. If the fragmented message was received on a temporary address, then the appropriate DTA bit should also be set in the AFM packet.
   b) If this is the first fragment of a fragmented message (C is set and no fragmented messages are in progress for this address and message number), then the host does not decrement the AFM counter and expects further fragments to be received for this address in subsequent frames.
   c) If this is the second or subsequent fragment of a fragmented message and further fragments will follow, (C is set and a fragmented message is in progress for this address and message number), then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set.
   d) If this is the last fragment of a fragmented message, (C is clear and a fragmented message is in progress for this address and message number), then the host decrements the AFM counter by 2, sending 2 AFM packets to the PCD5008 with the DAF bit set. If the fragmented message was received on a TA, then one of these AFM packets should also have the appropriate DTA bit set.
4. If, on receiving a status packet, the host determines that more than 32 or 128 frames have elapsed since the reception of a fragment for a fragmented message then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set. If the fragmented message was received on a TA, then the appropriate DTA bit should also be set in the AFM packet.
5. When no fragmented messages are in progress (the AFM counter = 0) and no TAs are pending (all TA counters = 0) and the FAF bit is clear in the AFM packet, the PCD5008 leaves AFM.

As an alternative to the above scheme, the host may choose to decrement the AFM counter at the end of the entire message by decrementing it once for each fragment received. This method is limited to a maximum of 127 fragments.

Tables 57 and 58 show examples of message reception with and without message fragmentation.

Table 57 Alphanumeric message without fragmentation

PACKET		PHASE	AFM COUNTER	COMMENT
NUMBER	TYPE			
1st	address 1	A	0	address 1 is received
2nd	vector 1	A	1	vector = alphanumeric type
3rd	message	A	1	message word received; C bit = 0; no more fragments are expected
4th	AFM		0	host writes AFM packet to the PCD5008 with the DAF bit = 1

Table 58 Alphanumeric message with fragmentation

PACKET		PHASE	AFM COUNTER	COMMENT
NUMBER	TYPE			
1st	address 1	A	0	address 1 is received
2nd	vector 1	A	1	vector = alphanumeric type
3rd	message	A	1	message word received; C bit = 1; message is fragmented, more expected
4th	status		1	end of frame indication (EOF = 1)
5th	address 1	B	1	address 1 is received
6th	vector 1	B	2	vector = alphanumeric type
7th	message	B	2	message word received; C bit = 1; message is fragmented, more expected
8th	AFM		1	host writes AFM packet to the PCD5008 with the DAF bit = 1
9th	status		1	end of frame indication (EOF = 1)
10th	address 1	A	1	address 1 is received
11th	vector 1	A	2	vector = alphanumeric type
12th	message	A	2	message word received; C bit = 0; no more fragments are expected
13th	AFM		1	host writes AFM packet to the PCD5008 with the DAF bit = 1
14th	AFM		0	host writes AFM packet to the PCD5008 with the DAF bit = 1

8.8.5.1 Fragmentation of non-7-bit character sets

FLEX™ alphanumeric messages can be used to send symbolic characters like Chinese, Kanji, etc. In this case several ASCII characters are used to represent each symbolic character. Enhanced fragmentation (EF) rules are provided by FLEX™ to allow character positions within a fragment to be determined in the event of missing fragments under poor signal conditions:

1. The pager must remove <NUL> characters from the end of fragments (where they are used as fill characters) so that the displayed message is not affected. To determine character boundaries, <NUL> (00H) characters in all other positions must be considered a result of channel errors. This allows each fragment to end with a complete character and does not disrupt pagers which do not follow all the EF rules.
2. The last fragment of a message containing symbolic characters is completed by filling unused character positions with <ETX> (03H) characters or <NUL> characters. When a message ends at exactly the last character position of the last BCH codeword, no additional <ETX> is required.
3. The U and V bits (Table 45) which aid decoding, are available in all fragments following the initial fragment. In the first fragment the message starts in the default character mode (U and V = 10). For subsequent fragments the definition of the U and V field is as shown in Table 59. When the U and V field is 00, characters may be split between fragments. When the U and V field is not 00, each fragment starts on a character boundary with the character mode defined as in Table 59.

8.8.6 MESSAGE CHECKSUMS

FLEX™ provides a message checksum facility for alphanumeric, numeric, hex/binary, and secure messages. The checksum is calculated by summing the information bits of each codeword in the message or message fragment (including control information and termination characters and bits in the last message codeword). Information bits of each codeword are broken into three groups as indicated in Table 60. Bits i_0, i_8 and i_{16} are the LSBs of each group and bit i_0 is the first bit of the codeword to be transmitted. The 3 groups are for each codeword are added to form a binary sum. The message checksum is the 1's complement of the LSBs of the binary sum, where the number of bits taken is determined by the message type (Section 8.7.8).

In the case of the 6-bit message checksum used in numeric messages, a binary sum is first calculated as described above. The binary sum is then truncated to its 8 LSBs, then the 2 MSBs are shifted right by 6 bits and added to the least significant 6 bits to form a new binary sum. The 6 LSBs of this new sum are taken and 1's complemented to form the 6-bit message checksum.

8.8.7 MESSAGE NUMBERING

FLEX™ messages may be numbered (Section 8.7.8), in this case the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in numerical order. The maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. When a message number is missed, the subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval.

Messages which can be received out of sequence are indicated by clearing the message retrieval flag R. Messages with R cleared number should not be included in the missed message calculation.

In case of fragmented messages, this number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.

Table 59 Fragmentation control bit definitions

U_0	V_0	DEFINITION
0	0	EF not supported in controller
0	1	reserved (for a second alternate character mode)
1	0	default character mode start position 1
1	1	alternate character mode start position 1

Table 60 Bit groups for message checksums

i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
group 1								group 2								group 3				

9 LIMITING VALUES

In accordance with the absolute maximum rating system (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–0.5	+5.0	V
I_{DD}	supply current		–	50	mA
I_I	DC input current (any input)		–10	+10	mA
I_O	DC output current (any output)		–10	+10	mA
V_I	input voltages (all inputs)	note 2	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation		–	300	mW
P_O	power dissipation per output		–	10	mW
T_{amb}	operating ambient temperature		–25	+70	°C
T_{stg}	storage temperature		–65	+150	°C

Notes

1. V_{DD1} and V_{DD2} respectively V_{SS1} and V_{SS2} must be connected at the same potential.
2. $V_{I(max)}$ = 5.0 V.

10 DC CHARACTERISTICS

T_{amb} = –25 to +70 °C; V_{DD} = 2.2 V; f = 76.8 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.8	2.2	3.6	V
$I_{DD(stby)}$	standby supply current	on = 0; note 1	–	4.2	10	μA
I_{DD}	operating supply current	on = 1; note 2	–	4.4	–	μA
Digital inputs: OSCPD, TEST2, TEST3, $\overline{\text{RESET}}$, LOBAT, EXTS0, EXTS1, $\overline{\text{SS}}$ and MOSI						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD}$	–	–	V
I_{LI}	LOW/HIGH-level input leakage current		–	–	1	μA
Digital outputs: MISO, $\overline{\text{READY}}$, CLKOUT, SYMCLK and S0 to S7						
V_{OL}	LOW-level output voltage	I_{sink} = 0.8 mA	–	0.1	0.4	V
V_{OH}	HIGH-level output voltage	I_{source} = –0.8 mA	V_{DD} – 0.4	V_{DD} – 0.1	–	V
I_{LO}	LOW/HIGH-level output leakage current	3-state outputs	–	–	1	μA

Notes

1. External clock signal (frequency = 76.8 kHz, amplitude = V_{SS} to V_{DD}) at pin EXTAL; OSCPD = HIGH; test inputs = LOW; other inputs = HIGH; outputs unconnected (note that any additional capacitive load at pin CLKOUT increases the supply current); SPI transmit enabled; to obtain the supply current of an application with a crystal connected as in Fig.18, a typical oscillator current of 2 μA needs to be added to this value (see Chapter 12); T_{amb} = 25 °C.
2. As note 1, but PCD5008 configured via SPI and synchronous to a typical FLEX™ data stream (collapse value = 4), T_{amb} = 25 °C.

11 AC CHARACTERISTICS

T_{amb} = −25 to +70 °C, V_{DD} = 1.8 to 3.6 V, f_{EXTAL} = 76.8 kHz, maximum load capacitance = 50 pF connected to any digital output; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset timing						
$t_{W(rst)}$	$\overline{\text{RESET}}$ pulse width		200	–	–	ns
$t_{LH(RESET-READY)}$	$\overline{\text{RESET}}$ LOW to $\overline{\text{READY}}$ HIGH		–	–	200	ns
$t_{HL(RESET-READY)}$	$\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW	stable 76.8 kHz clock	–	1	–	s
Start-up timing						
$t_{strt(osc)}$	oscillator start-up time	see Fig.18	–	1	–	s
$t_{h(rst)}$	$\overline{\text{RESET}}$ hold time		200	–	–	ns
$t_{HL(RESET-READY)}$	$\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW	note 1	–	76800	–	T
$t_{WUL(osc-READY)}$	oscillator warmed up to $\overline{\text{READY}}$ LOW		–	1	–	s
SPI timing						
f_{SCK}	operating frequency		0	–	1	MHz
$T_{cy(SCK)}$	cycle time		1000	–	–	ns
t_{LEAD1}	select lead time		200	–	–	ns
t_{LAG1}	de-select lag time		200	–	–	ns
$t_{d(SS-READY)}$	$\overline{\text{SS}}$-to-$\overline{\text{READY}}$ delay time	previous packet did not program an address word; note 2	–	–	80	µs
		previous packet programmed an address word; note 2	–	–	420	µs
t_{READYH}	$\overline{\text{READY}}$ HIGH time		50	–	–	µs
t_{LEAD2}	$\overline{\text{READY}}$ lead time		200	–	–	ns
t_{LAG2}	$\overline{\text{READY}}$ lag time		–	–	200	ns
$t_{su(i)(D)}$	MOSI data setup time		200	–	–	ns
$t_{h(i)(D)}$	MOSI data hold time		200	–	–	ns
$t_{ACC(o)}$	MISO access time		0	–	200	ns
$t_{o(dis)}$	MISO disable time		–	–	300	ns
t_{DOV}	MISO data valid time		–	–	200	ns
$t_{h(o)(D)}$	MISO data hold time		0	–	–	ns
t_{SSH}	$\overline{\text{SS}}$ HIGH time		200	–	–	ns
t_{SCKH}	SCK HIGH time		300	–	–	ns
t_{SCKL}	SCK LOW time		300	–	–	ns
t_r	SCK rise time	10% to 90% V_{DD}	–	–	1	µs
t_f	SCK fall time	10% to 90% V_{DD}	–	–	1	µs

Notes

1. T is one period of the 76.8 kHz clock source. Note that from power-up, the oscillator start-up time can influence the availability and period of clock strobes. This can affect the $\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW timing.
2. When the host re-programs an address word with a host-to-decoder packet ID > 7FH, there is an added delay before the PCD5008 is ready for another packet.

12 OSCILLATOR CHARACTERISTICS

T_{amb} = −25 to +70 °C; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_1	external capacitor at pin EXTAL	note 1	–	15	–	pF
C_2	external capacitor at pin XTAL	note 1	–	15	–	pF
R_f	external feedback resistor	note 1	–	10	–	MΩ
$g_{m(osc)}$	oscillator transconductance	V_{DD} = 1.8 V	9.4	19.6	–	µS
		V_{DD} = 3.6 V	–	22.6	50	µS
I_{osc}	oscillator operating supply current	V_{DD} = 2.2 V; note 2	–	2	–	µA

Notes

1. Designed for quartz crystal type: SEIKO VTC200 or equivalent; parameters: f = 76800Hz, R_S = 35 kΩ (max.), $C_L = (C_1//C_2) + C_{stray}$ = 8 to 12 pF, C_0 = crystal shunt capacitance = 0.8 pF (typ.), C_f = typical parasitic pin capacitance = 2 pF; maximum overall frequency tolerance (including transmitter) is 300 ppm (Section 8.4.4).
2. Extracted from evaluations under conditions as in Fig.18; this value is strongly dependent on external conditions (load and parasitic capacitances).

13 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

15 TEST AND APPLICATION INFORMATION

15.1 Example application

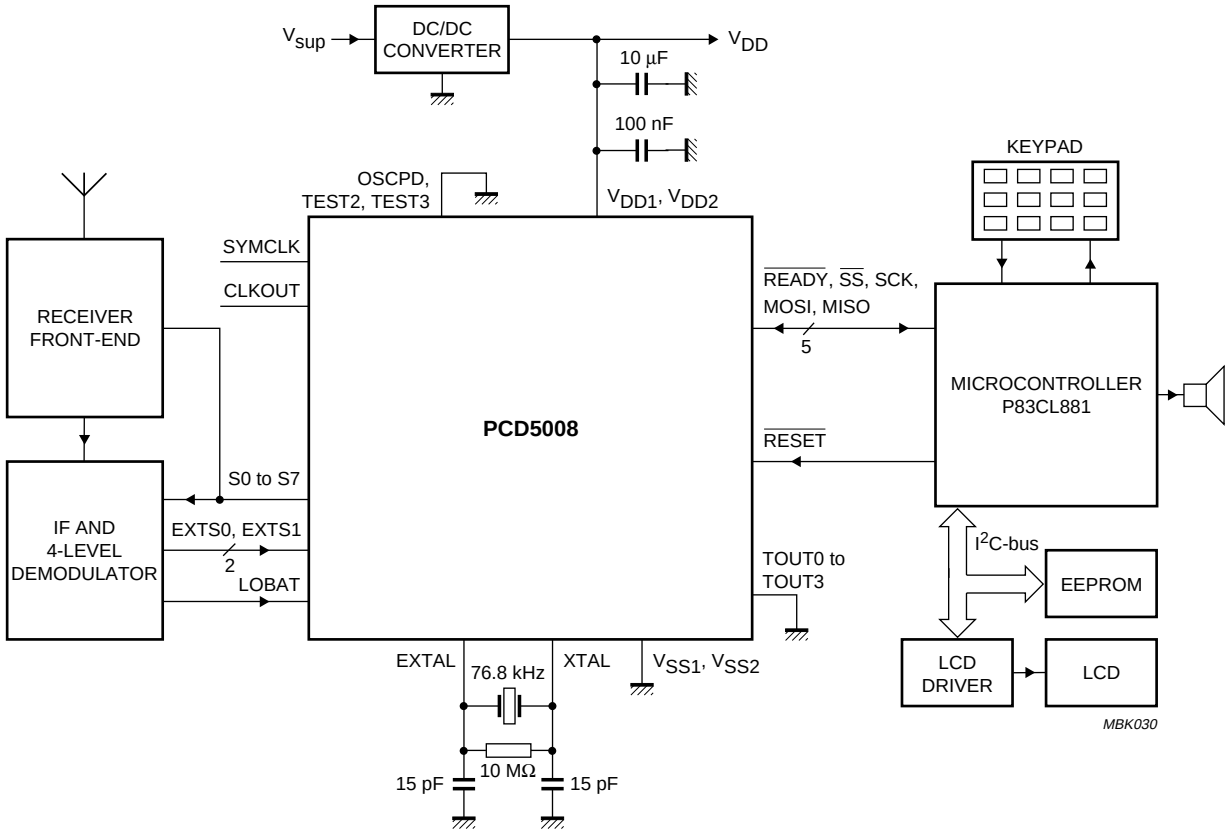


Fig.18 Example application.

15.2 System block diagram

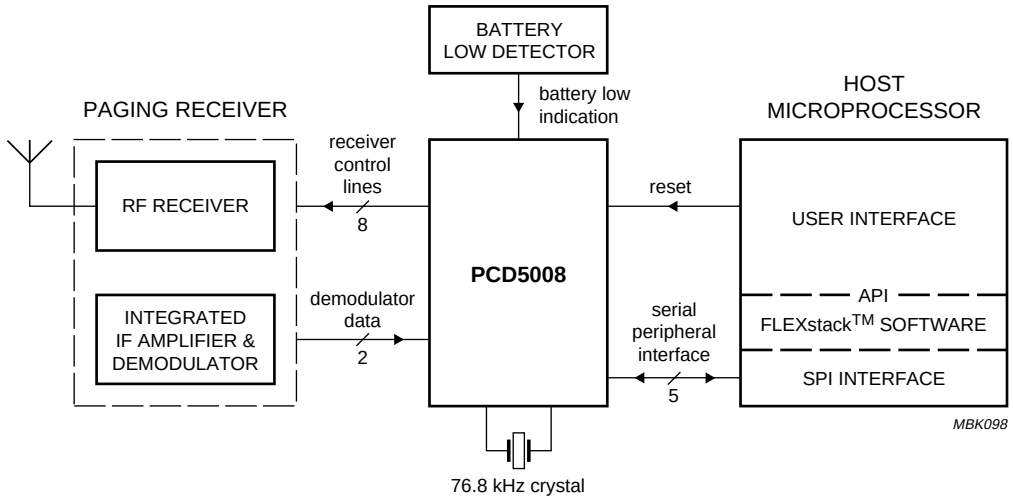


Fig.19 System block diagram.

15.3 FLEX™ encoding and decoding rules

The encoding and decoding rules identify the minimum requirements which must be met by the paging device, paging terminal or other encoding equipment to properly format a FLEX™ data stream for RF transmission and to successfully decode it.

15.3.1 FLEX™ ENCODING RULES

The FLEX™ encoding rules are as follows:

- The stability of the encoder clock used to establish time positions of FLEX™ frames must be no worse than ±25 ppm (including worst case temperature and aging effects).
- A maximum of 2 occurrences of an identical individual or radio group address is allowed in any frame for unfragmented messages. This rule applies across all phases in a multi-phase frame. For example, for decoding devices that support any-phase addressing, an any-phase address may appear at once in two different phases in a single multi-phase frame.
- Once an individual or radio group address is used to begin transmitting a fragmented message, that same address must not be used to start a new fragmented transmission until the first fragmented transmission has been completed.
- For the duration of time that an individual or radio group address is being used to send a fragmented message, that same address must not appear more than once in any frame to send an unfragmented message.
- Once a specific dynamic group address (temporary address) is assigned to a group, it must not be reused until its associated message has been transmitted in its entirety. Given this constraint, the same dynamic group address can only appear once in any frame.
- A dynamic group address cannot be used to set up a second dynamic group.
- Messages using any of the three defined numeric vectors ($V_2V_1V_0$ = 011, 100 and 111) cannot be fragmented, and thus must be completely contained in a single frame.
- Fragments of the same message must be sent at a frequency of at least 1 every 32 frames (i.e. at least once a minute) or 1 every 128 frames (i.e. at least once every 4 minutes) as specified by the service provider.
- Enhanced message fragmenting for symbolic character transmission requires that the encoder track character boundaries within each fragment in order to avoid character splitting.
- Message numbering as an optional feature is offered by some carriers and available on an individual subscriber basis.
- Message numbers must be assigned sequentially in ascending order.
- Message number sequences must be separately maintained for each individual and radio group address.
- Message numbers are not used (retrieval message number disabled) in conjunction with a dynamic group address.
- When a missed message is re-transmitted from message retrieval storage, the message must have R = 0 to avoid creating an out of sequence message which may cause the pager to indicate a missed message.

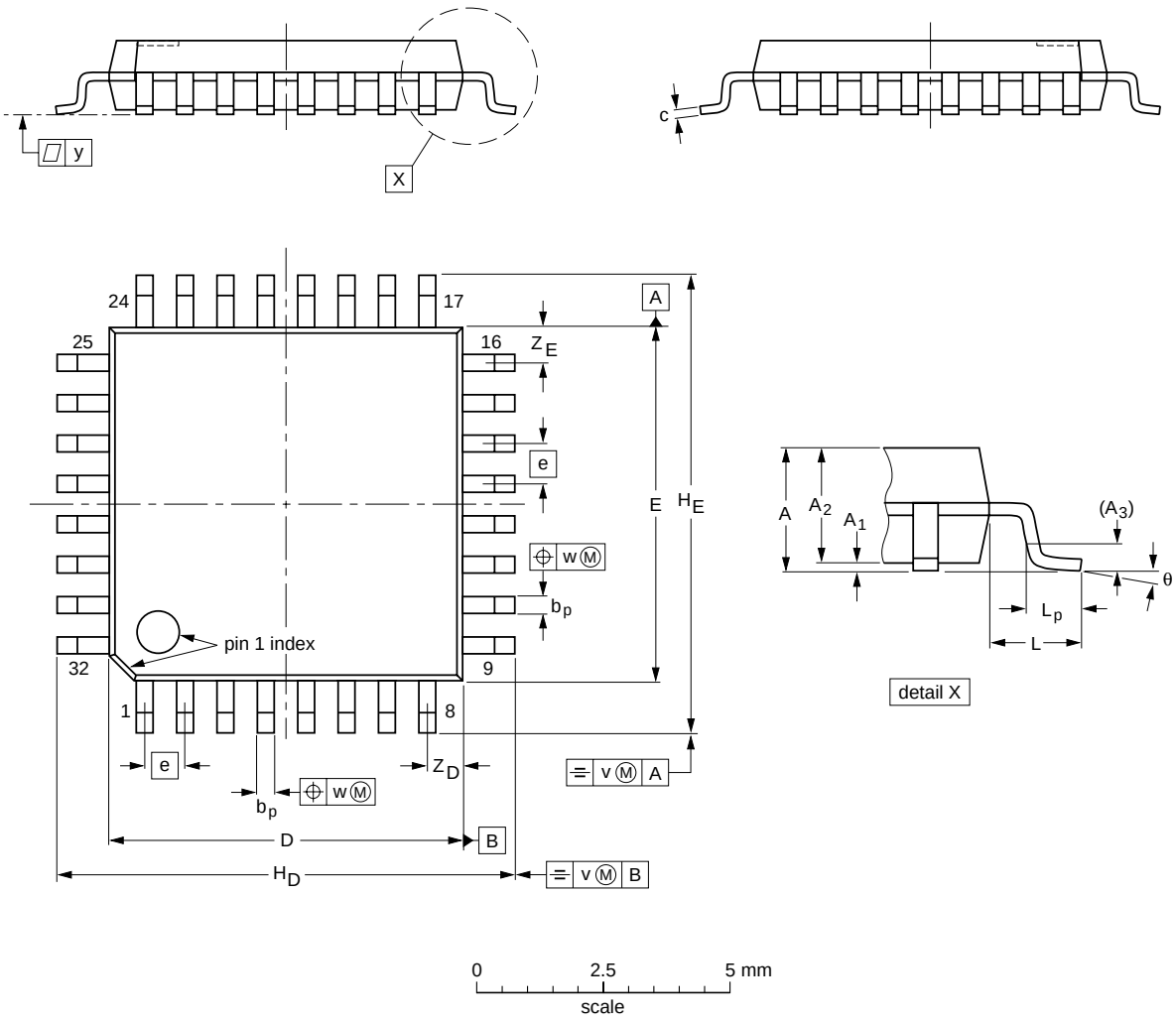
15.3.2 FLEX™ DECODING RULES

The FLEX™ decoding rules are as follows:

- FLEX™ decoding devices may implement either single-phase addressing or any-phase addressing.
- FLEX™ decoding devices that support the numeric vector type ($V_2V_1V_0$ = 011) must also support the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00.
- FLEX™ decoding devices that support the alphanumeric vector type ($V_2V_1V_0$ = 101) must support the numeric vector type ($V_2V_1V_0$ = 011) and the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00, FLEX™ paging devices that implement any-phase and support the alphanumeric vector type ($V_2V_1V_0$ = 101) must also support the short instruction vector ($V_2V_1V_0$ = 001) with the instruction type ($i_2i_1i_0$) set to 000.
- FLEX™ decoding devices must be capable of decoding frames at all of the following combinations of data rate and modulation mode. They are: 1600 bps 2 level; 3200 bps 2 level; 3200 4 level and 6400 bps 4 level.
- FLEX™ decoding devices must be designed to tolerate 4 minute fragment separation times.

16 PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~95-12-19~~ 97-08-04

17 SOLDERING

17.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

17.2 Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

17.3 Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

19 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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